

FIG. 1

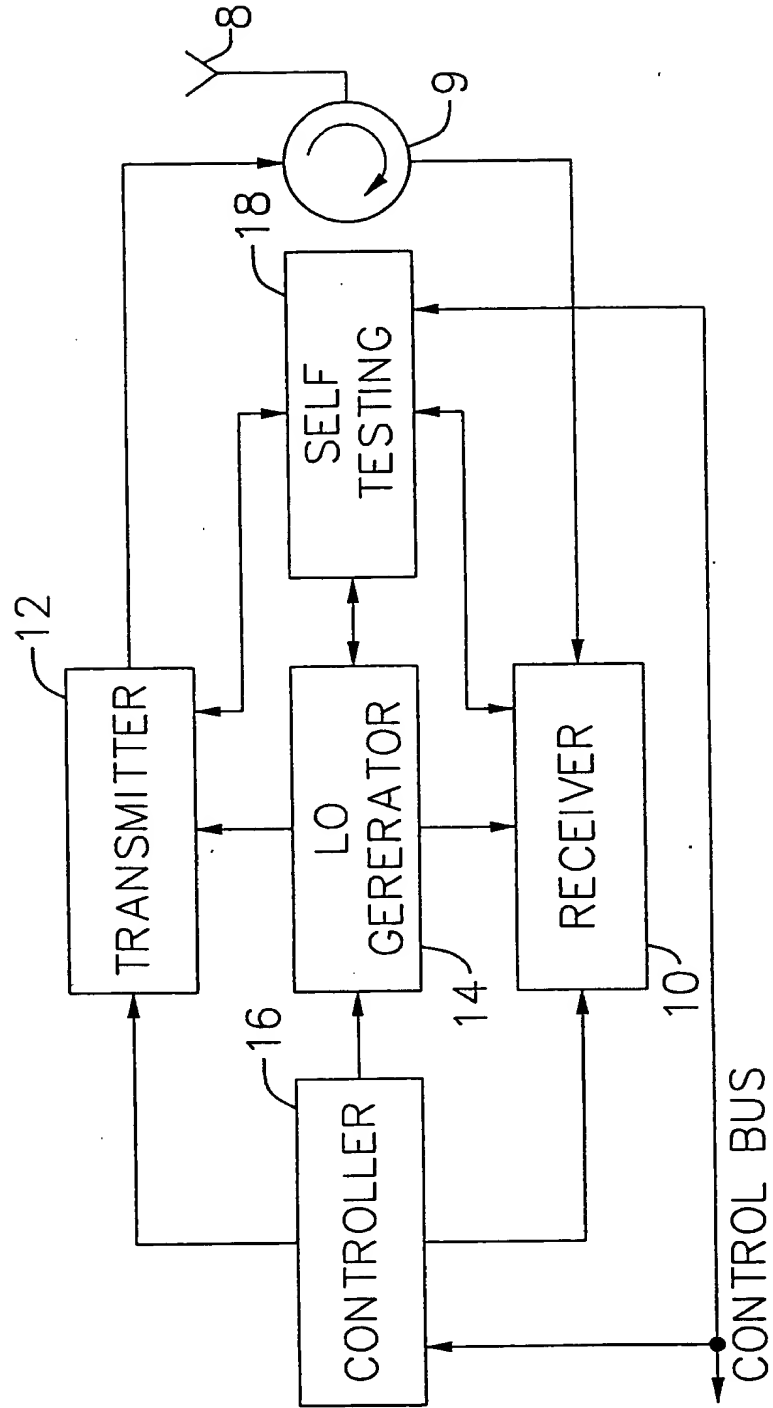


FIG. 2

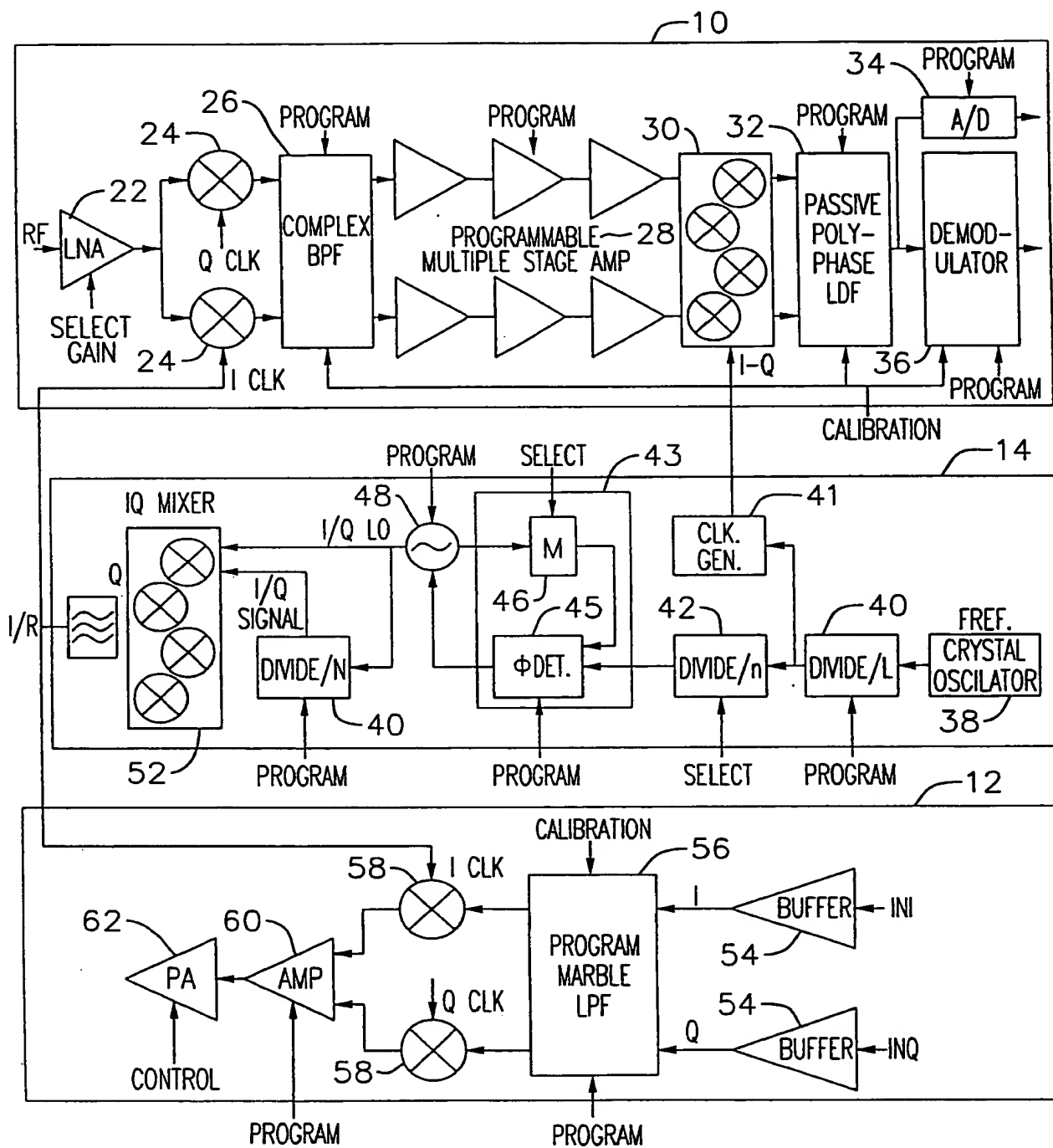


FIG. 3

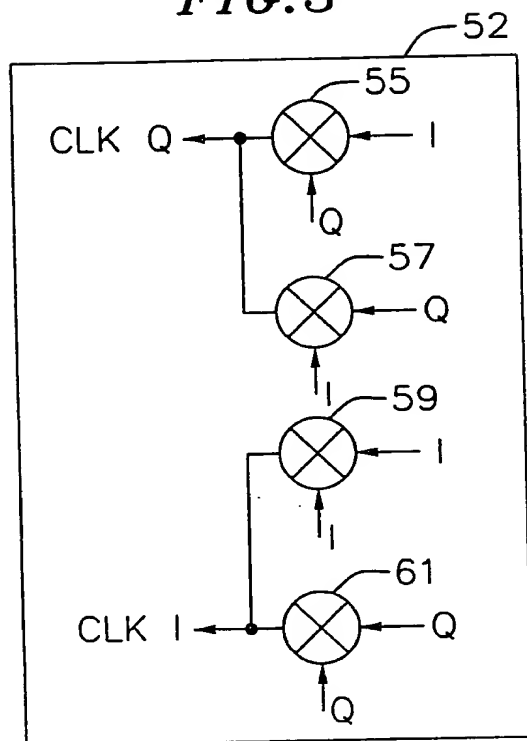
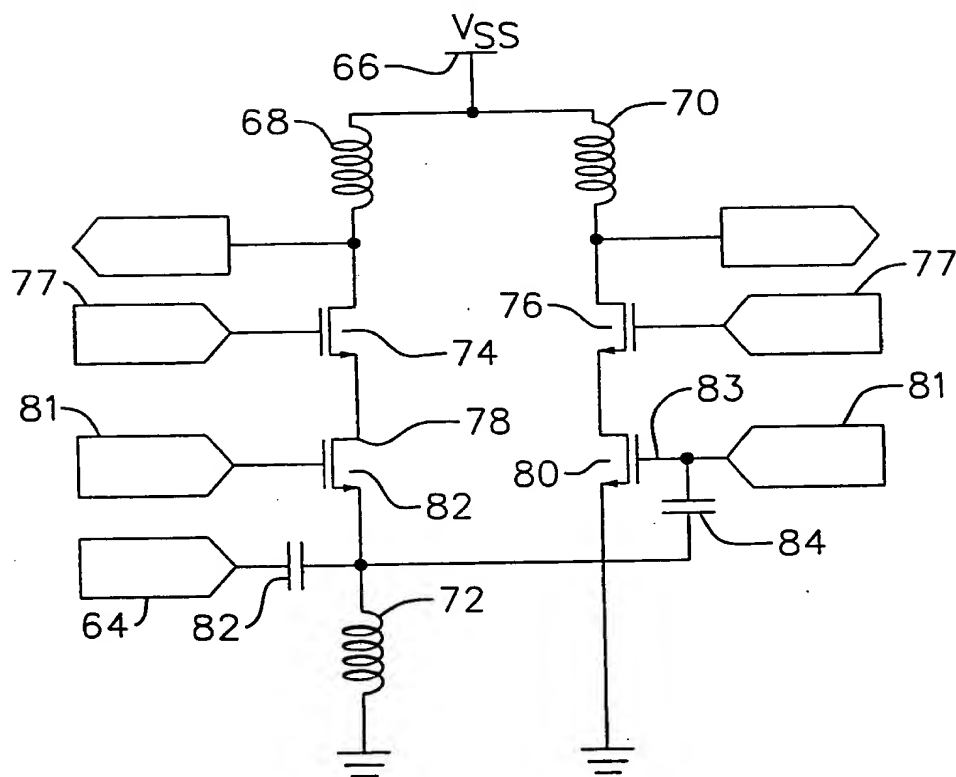


FIG. 4



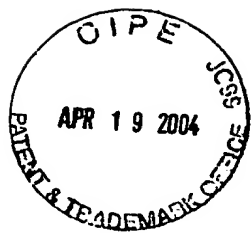


FIG. 4(a)

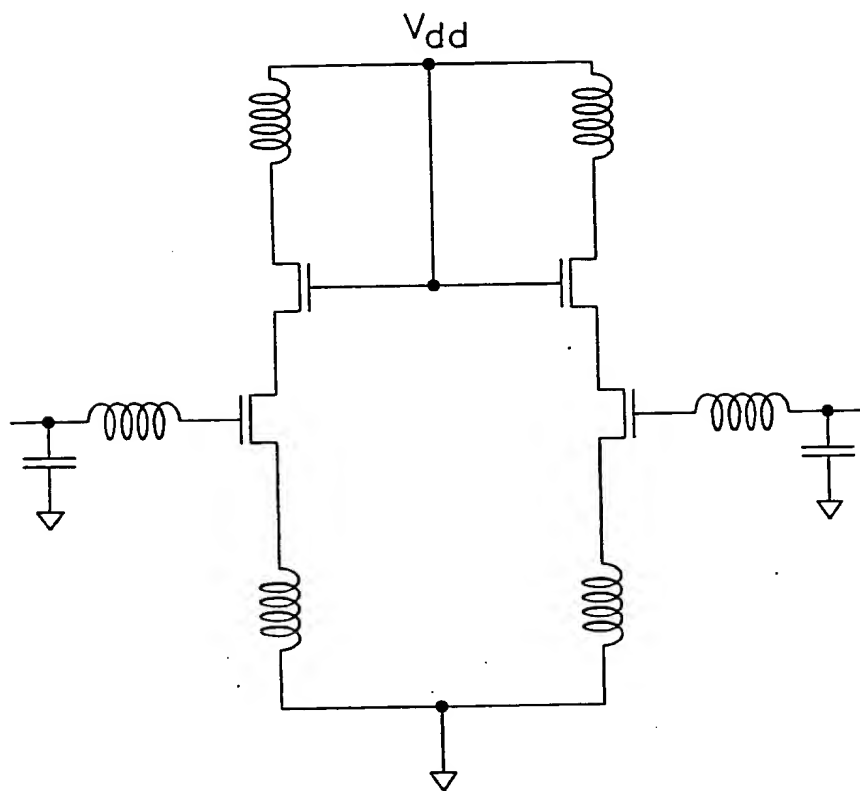


FIG. 5

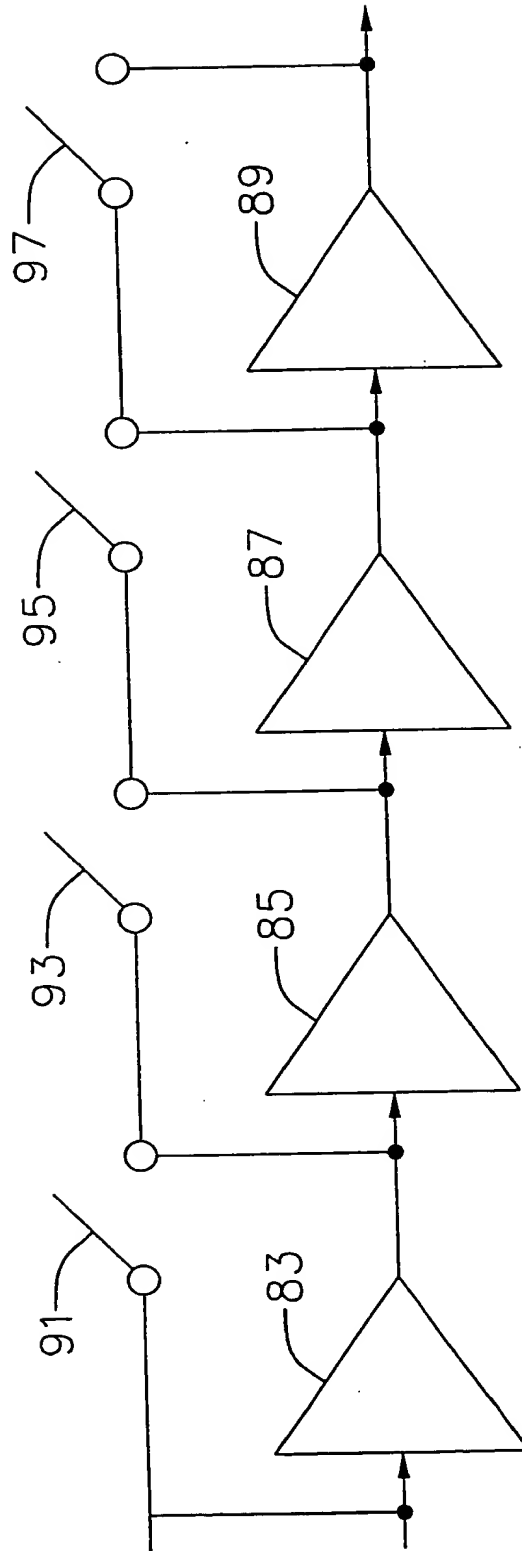


FIG. 6

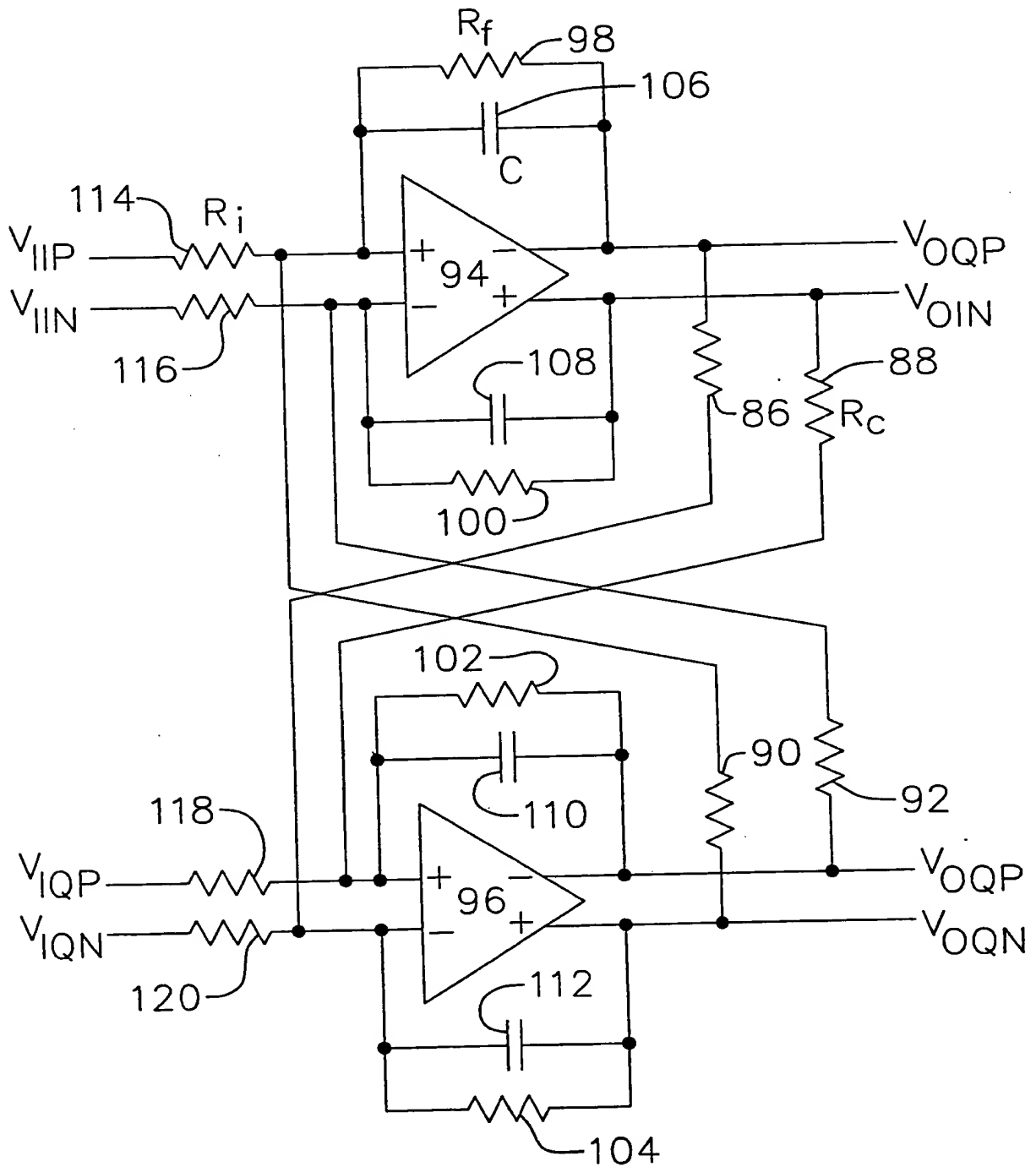


FIG. 7

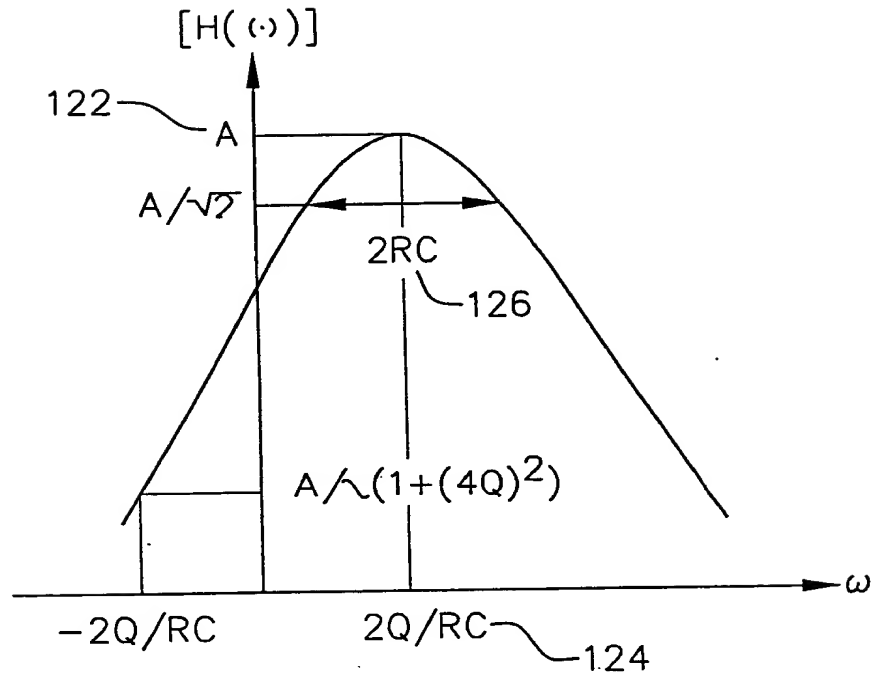


FIG. 8

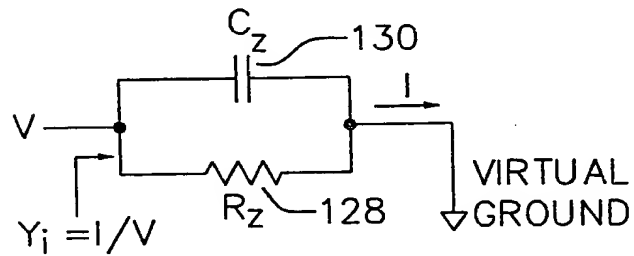


FIG. 9

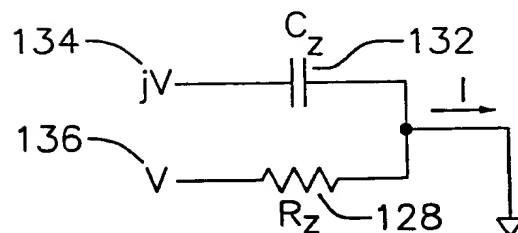


FIG. 10

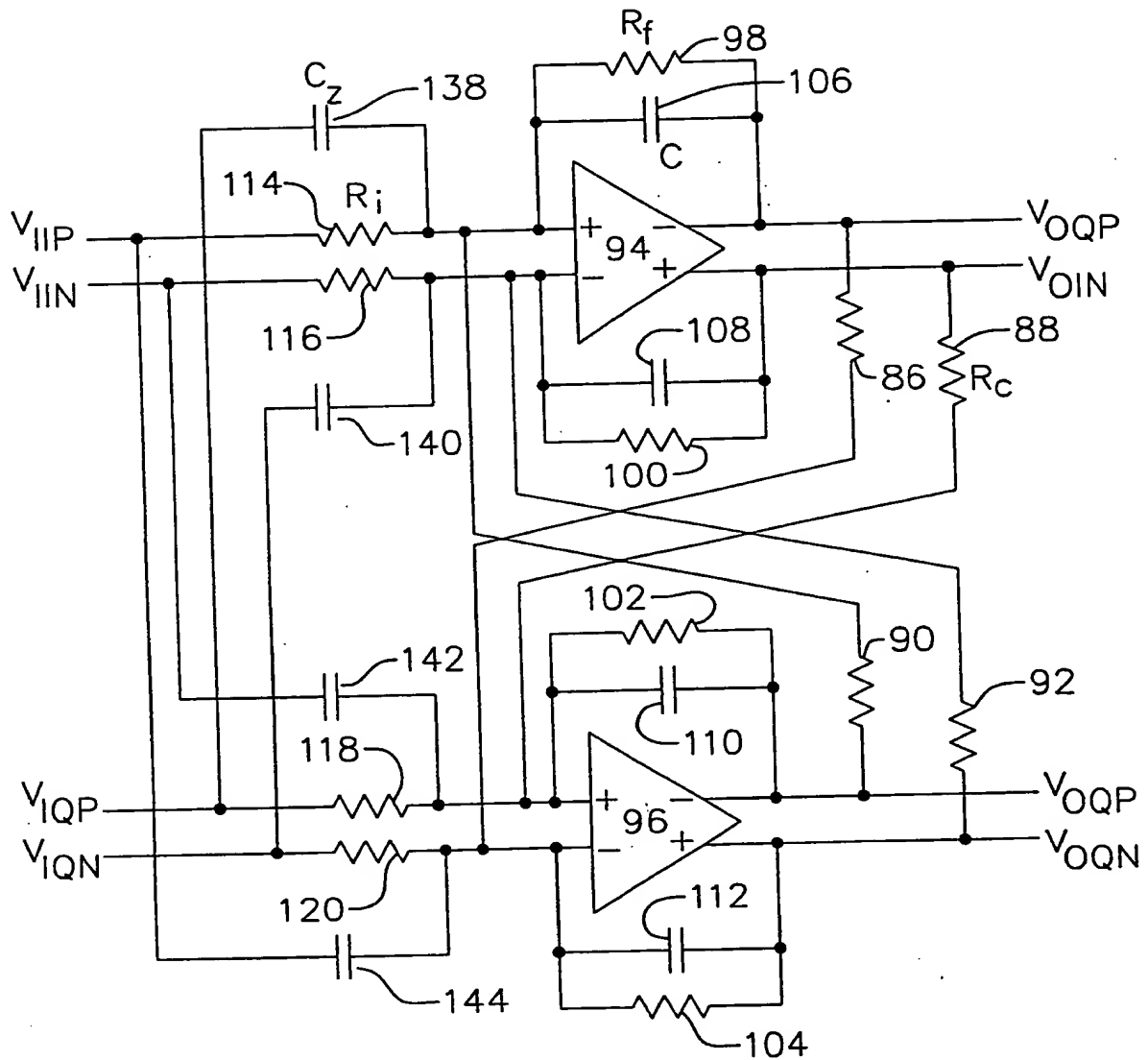




FIG. 11

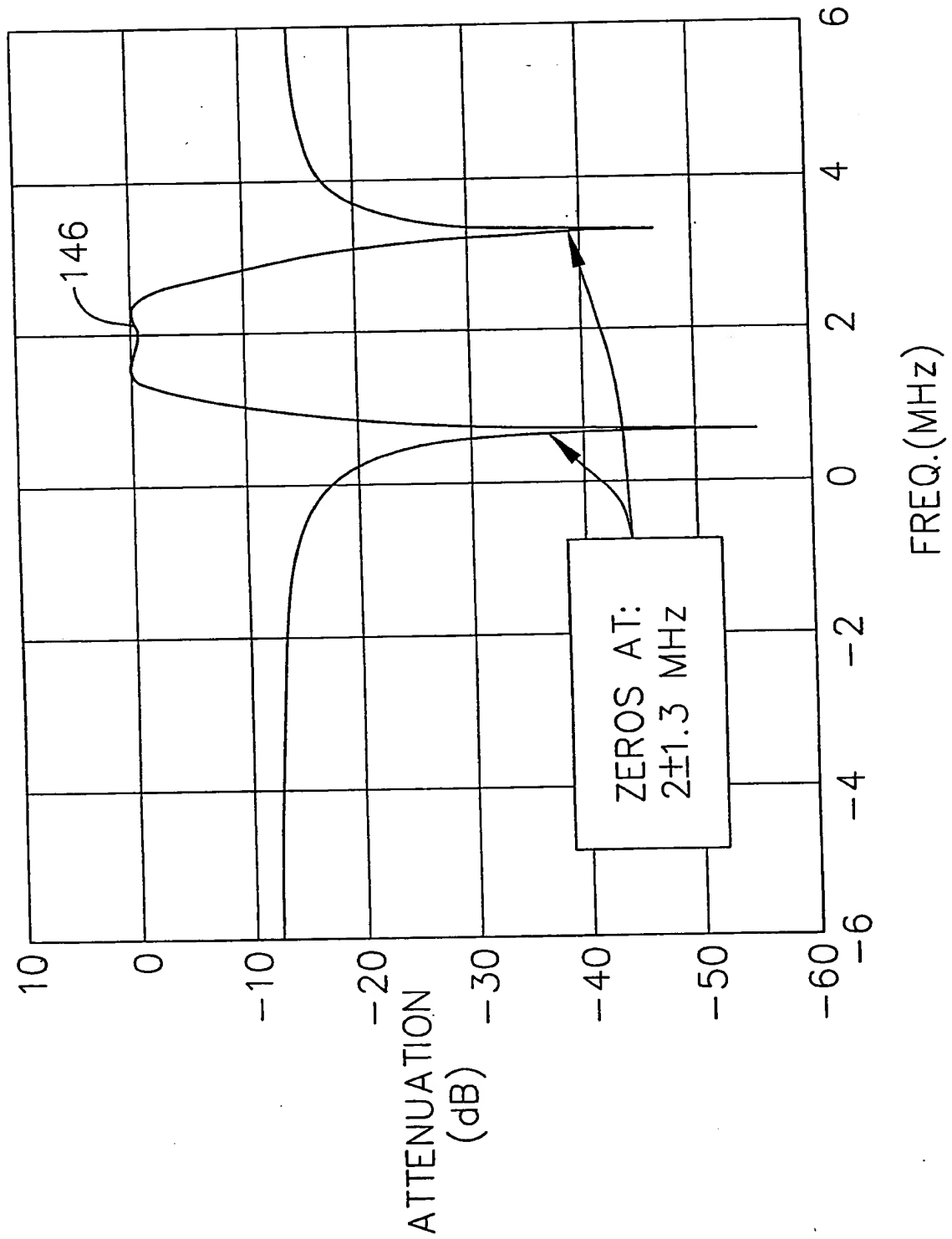


FIG. 12a

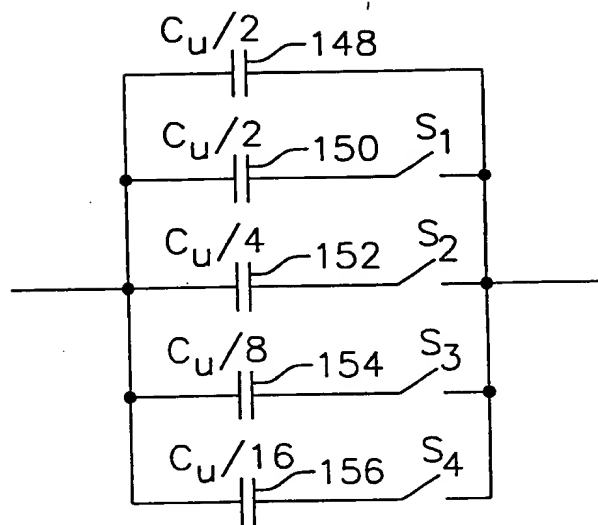


FIG. 12b

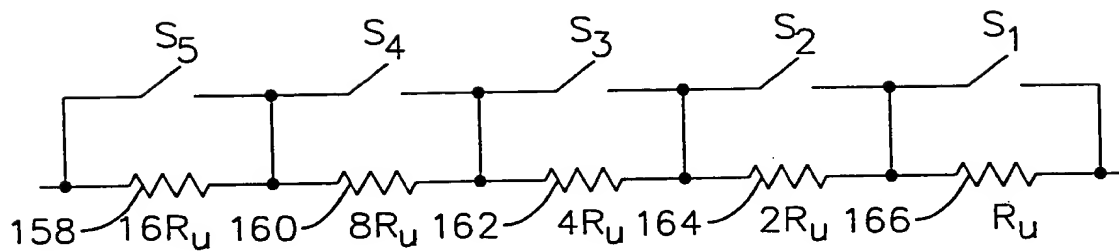


FIG. 13

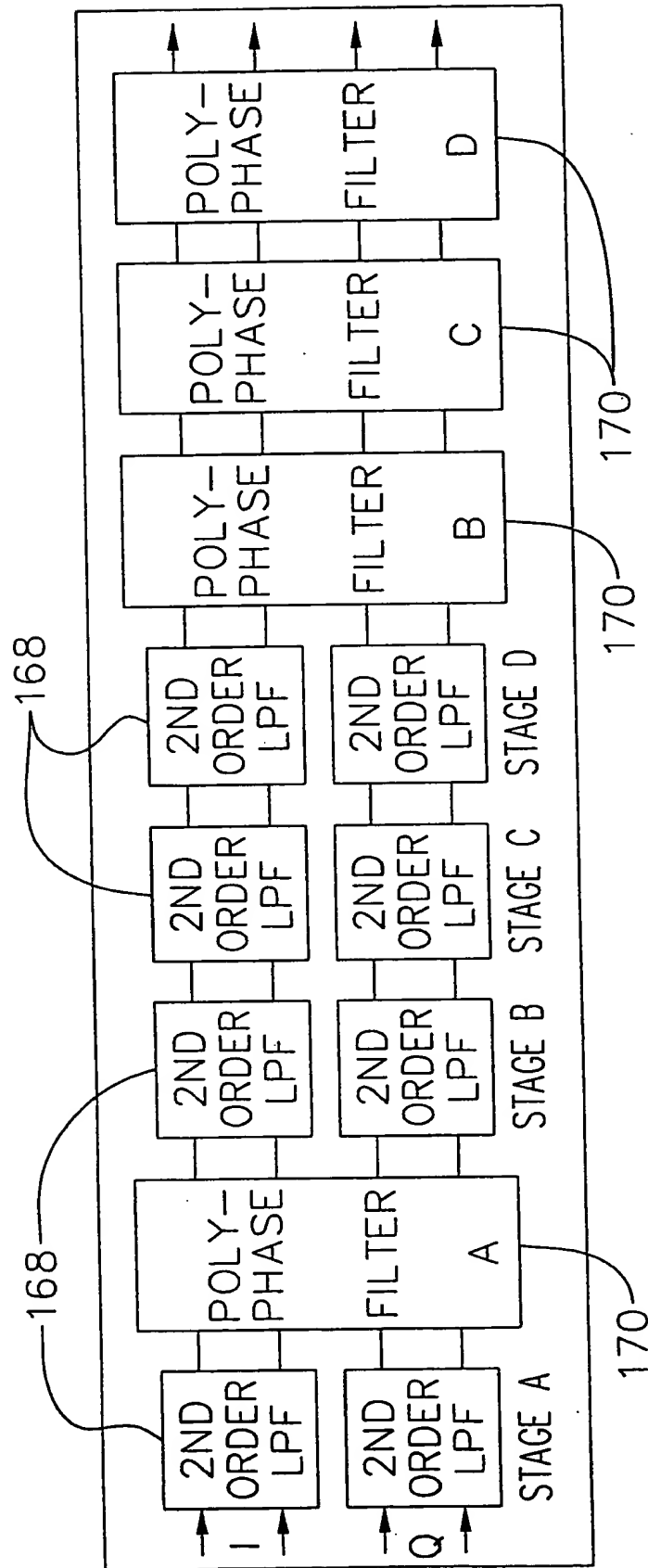
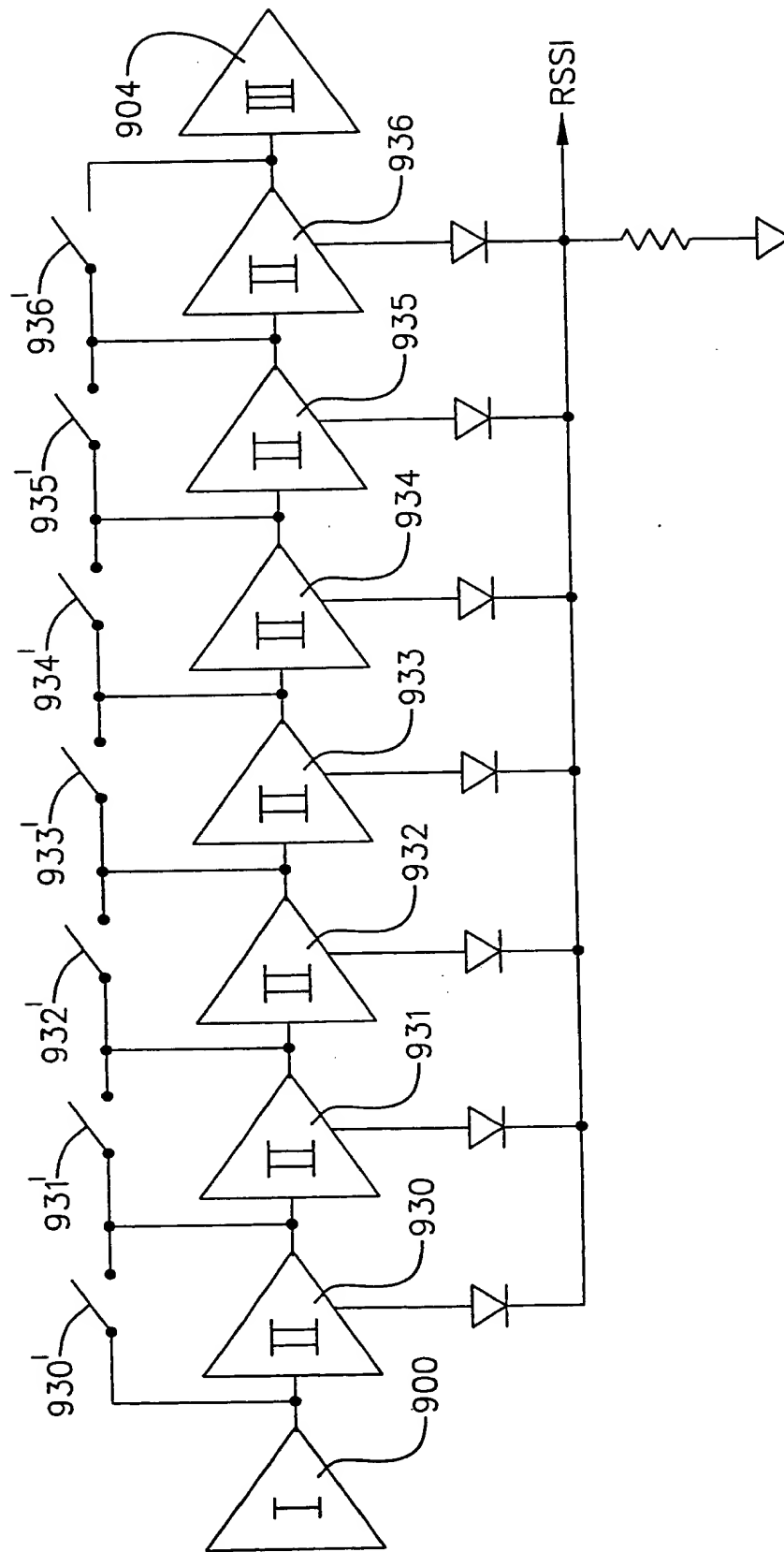


FIG. 14





[illegible]

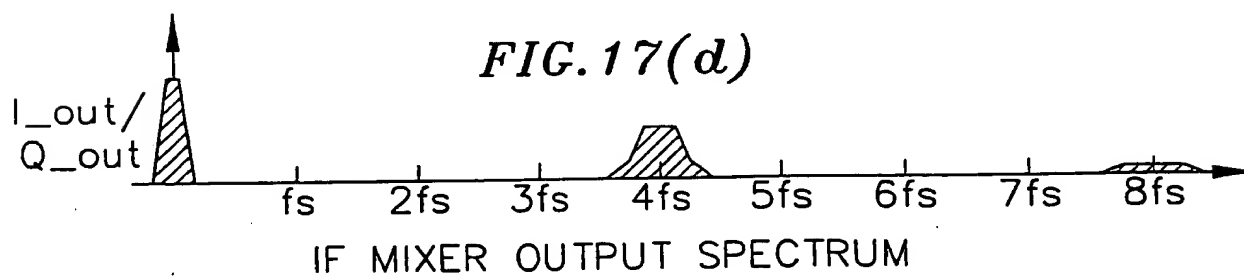
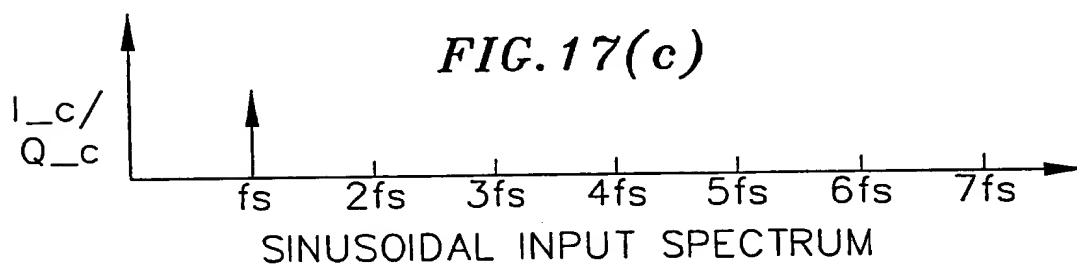
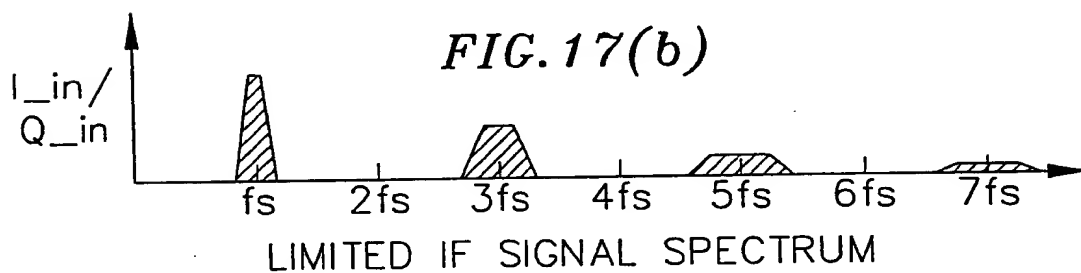
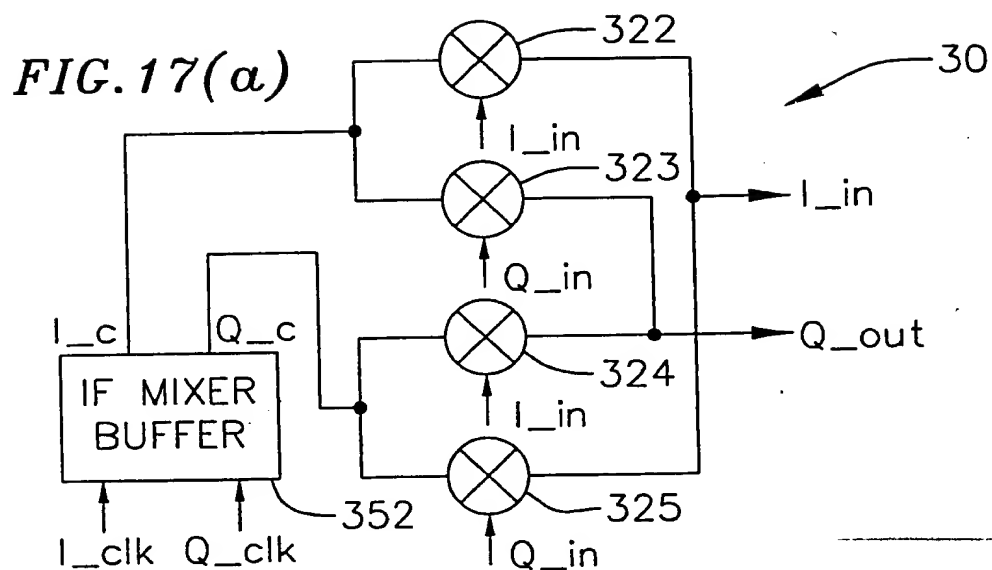


FIG. 18

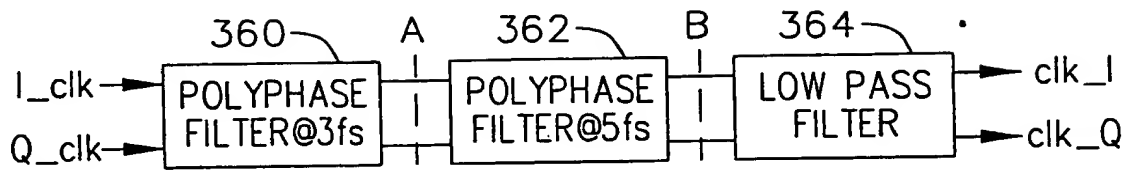


FIG. 19(a)

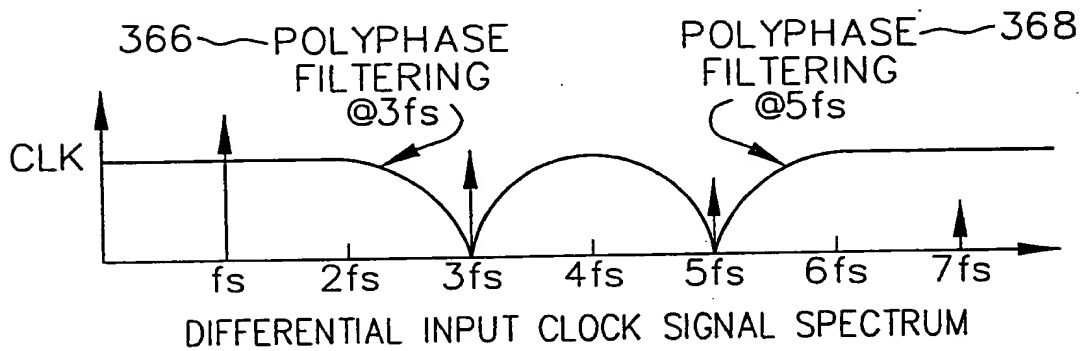


FIG. 19(b)

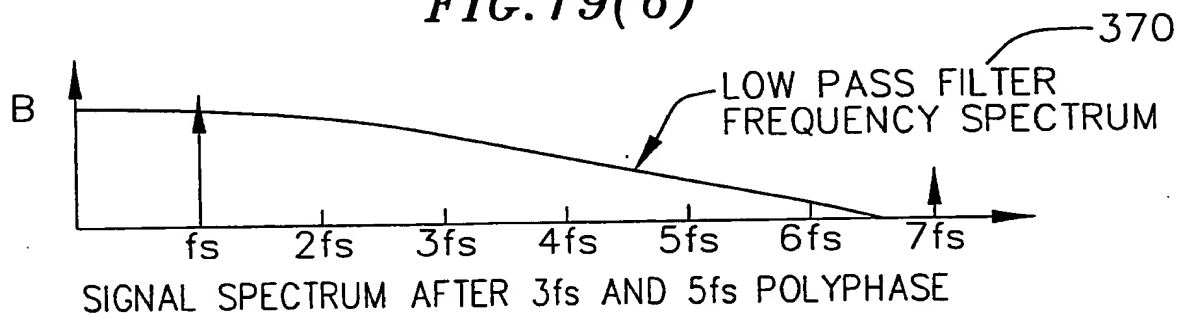
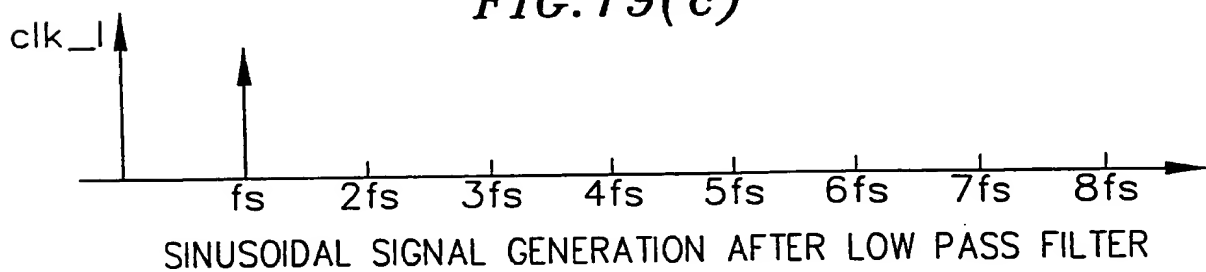


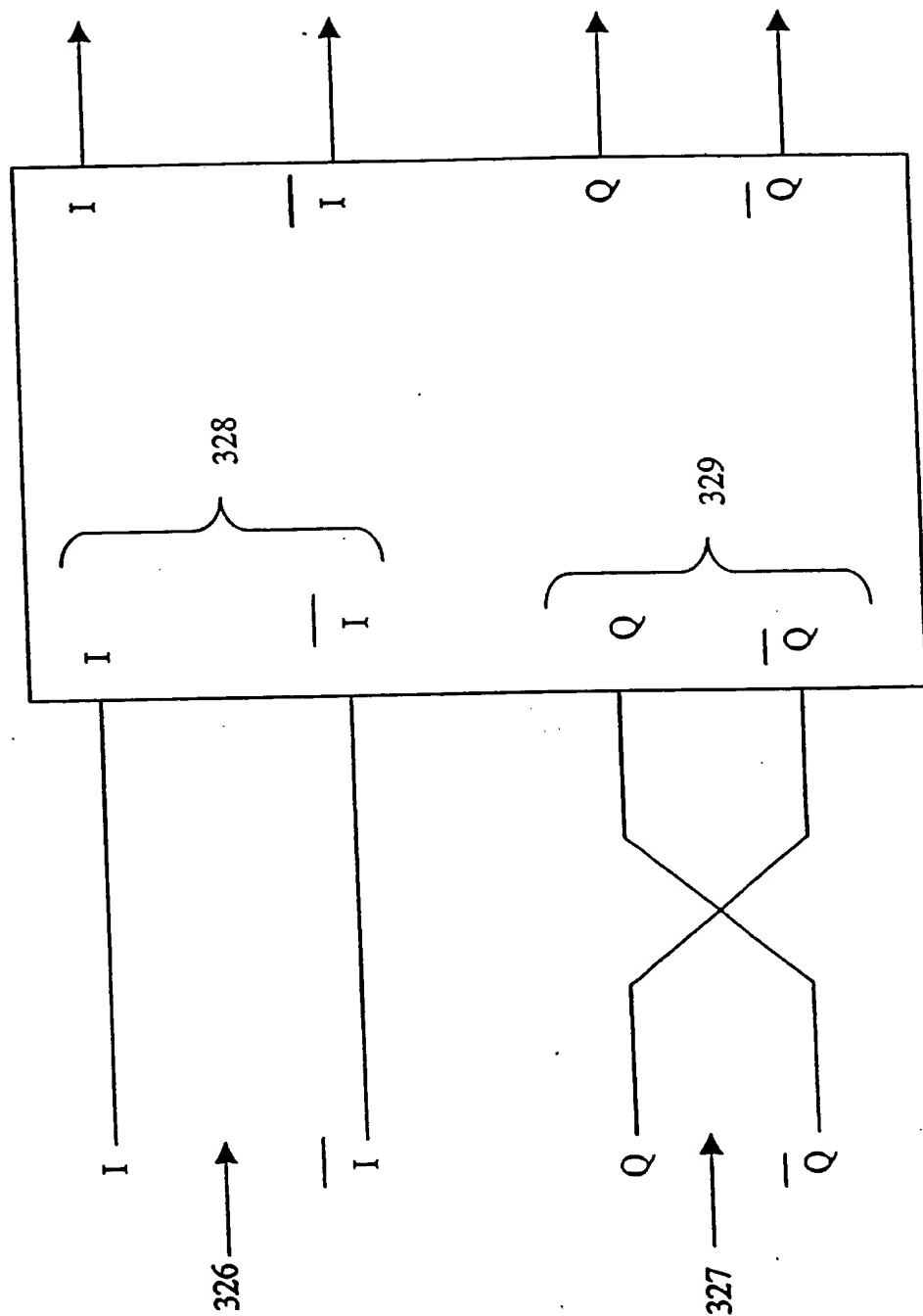
FIG. 19(c)

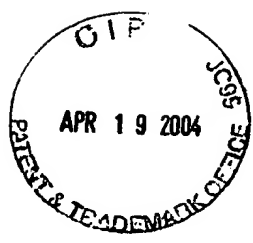




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FIG. 19d





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FIG. 19e

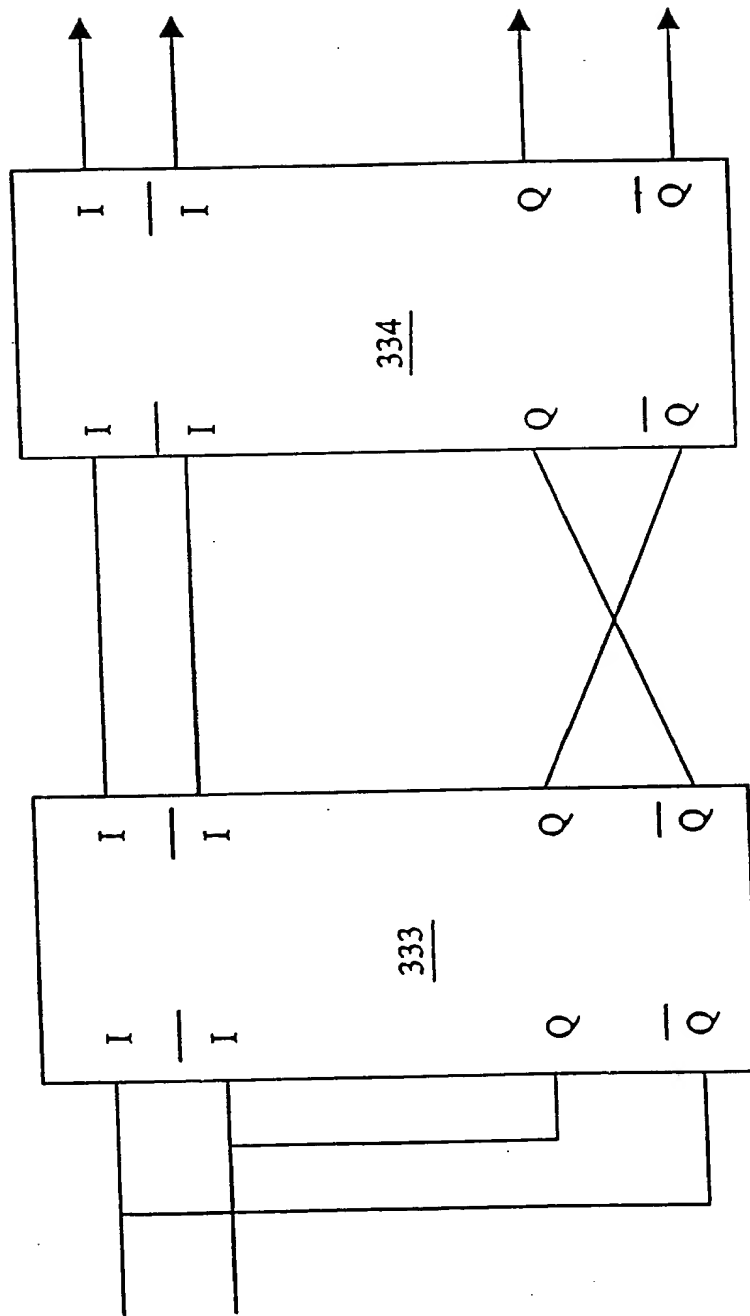


FIG. 19f

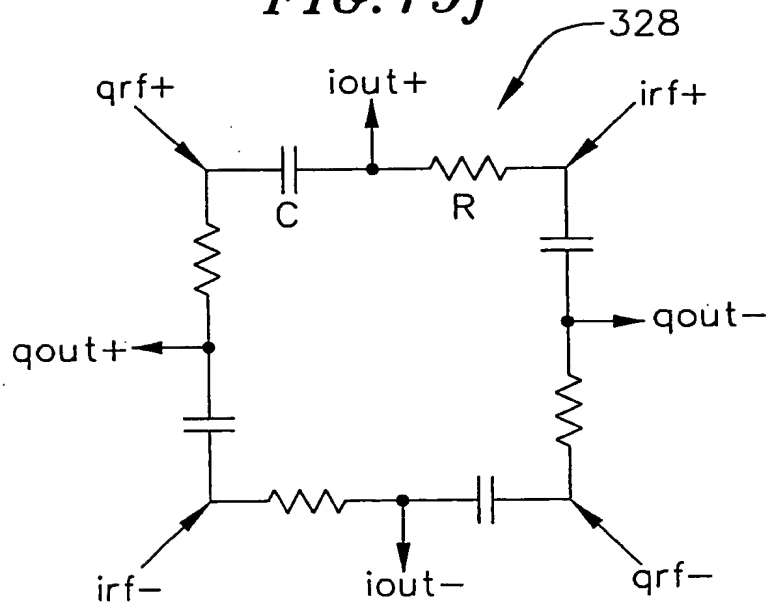
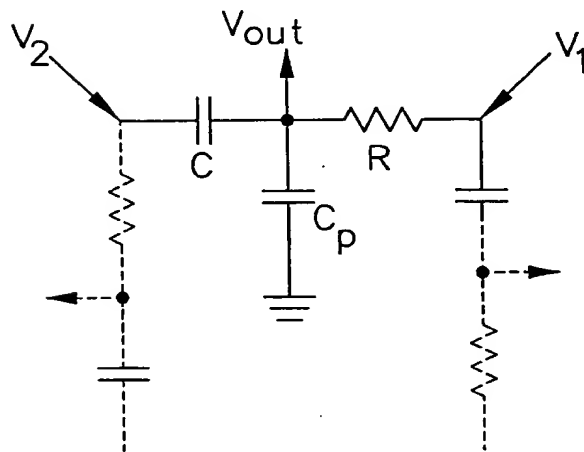


FIG. 19g



$$\omega_p = \frac{1}{R(C_p + C)}$$

$$\omega_o = \frac{1}{RC}$$

$$V_{out} = \frac{V_1}{R(C_p + C)s + 1} + \frac{V_2 RCs}{R(C_p + C)s + 1}$$

FIG.20(a)

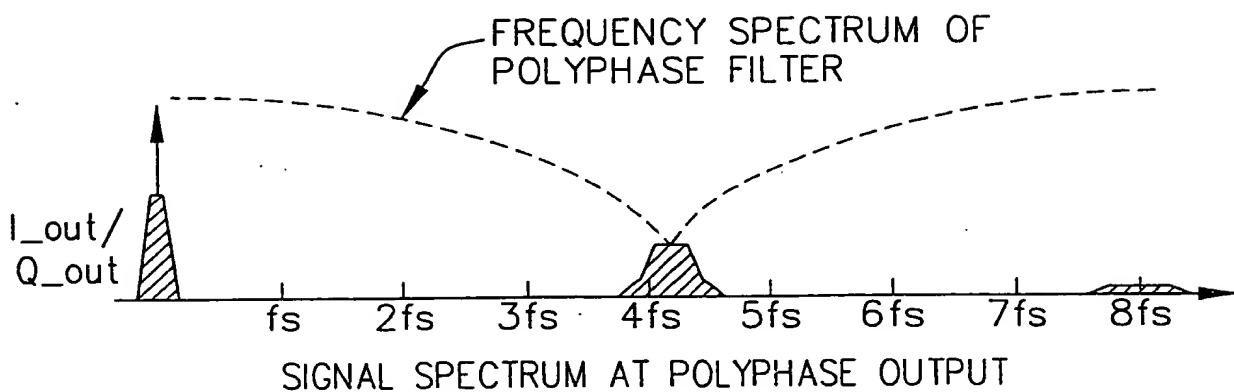


FIG.20(b)

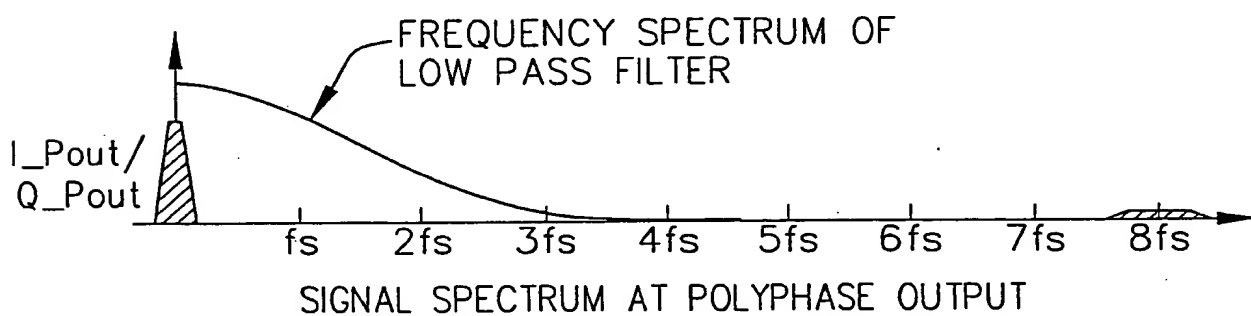


FIG.20(c)

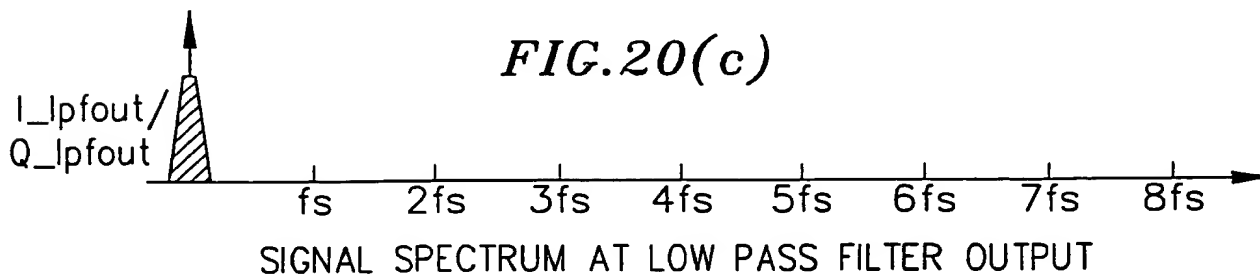


FIG. 21

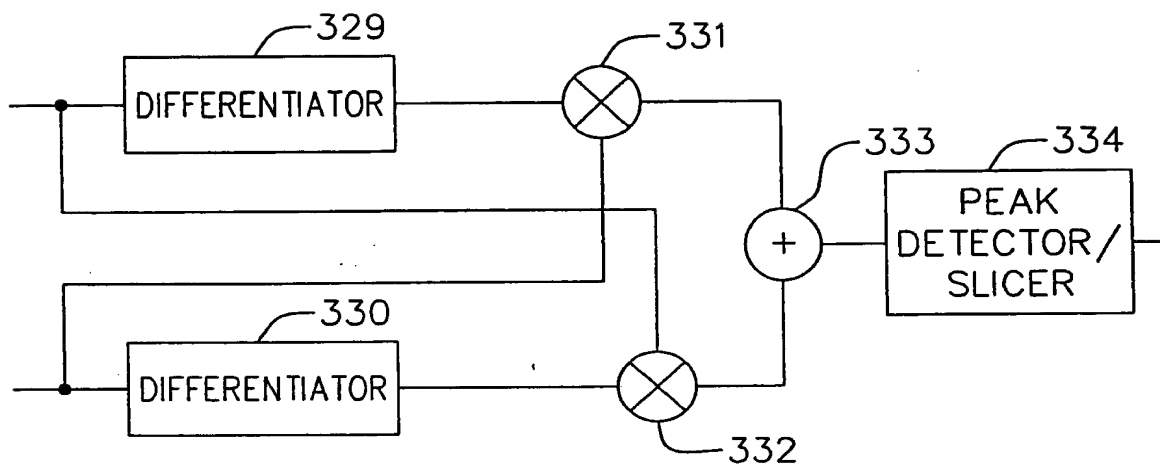


FIG. 22

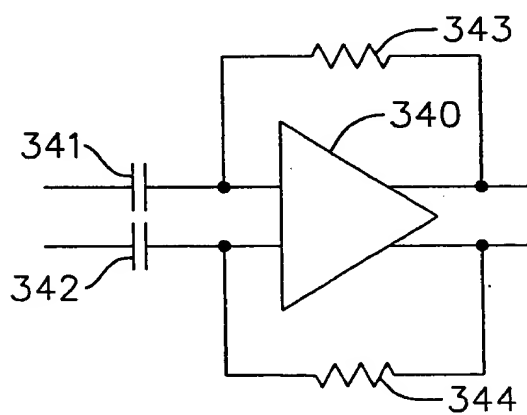


FIG. 23

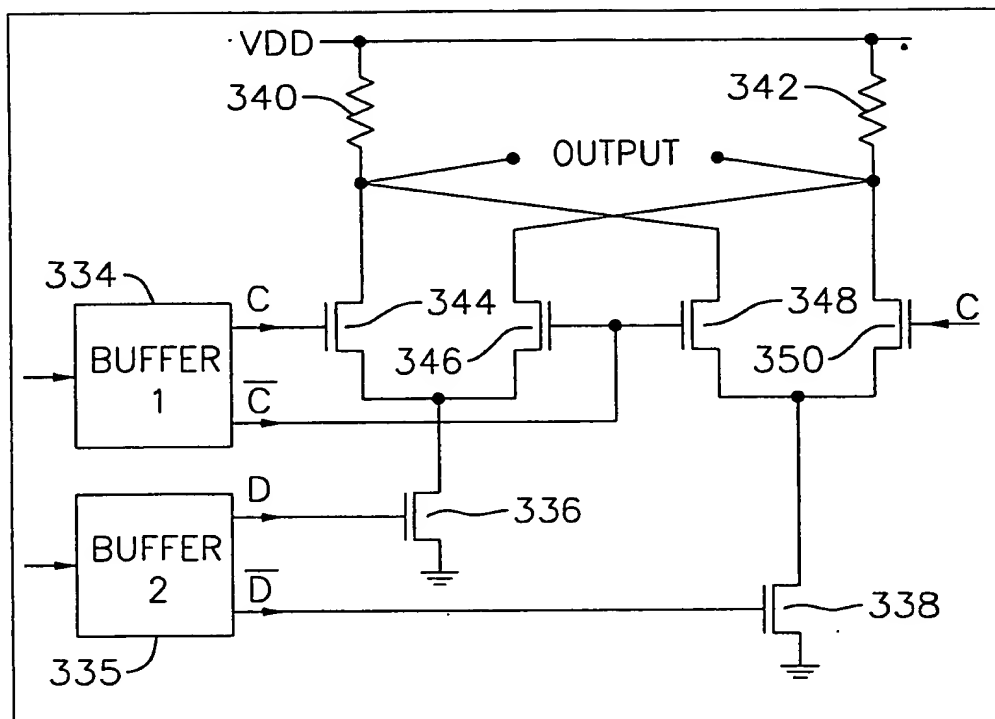


FIG. 24

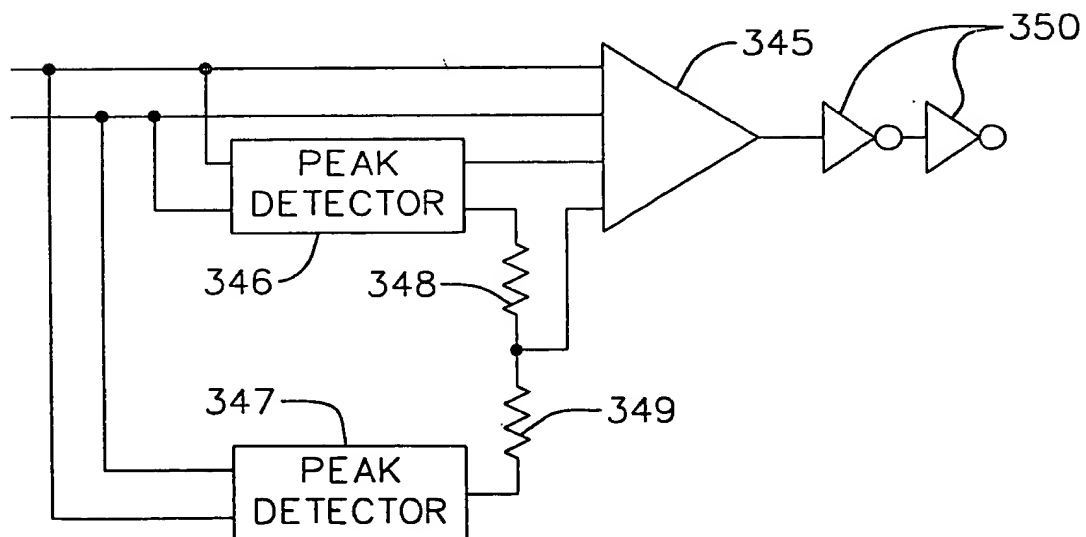


FIG. 25

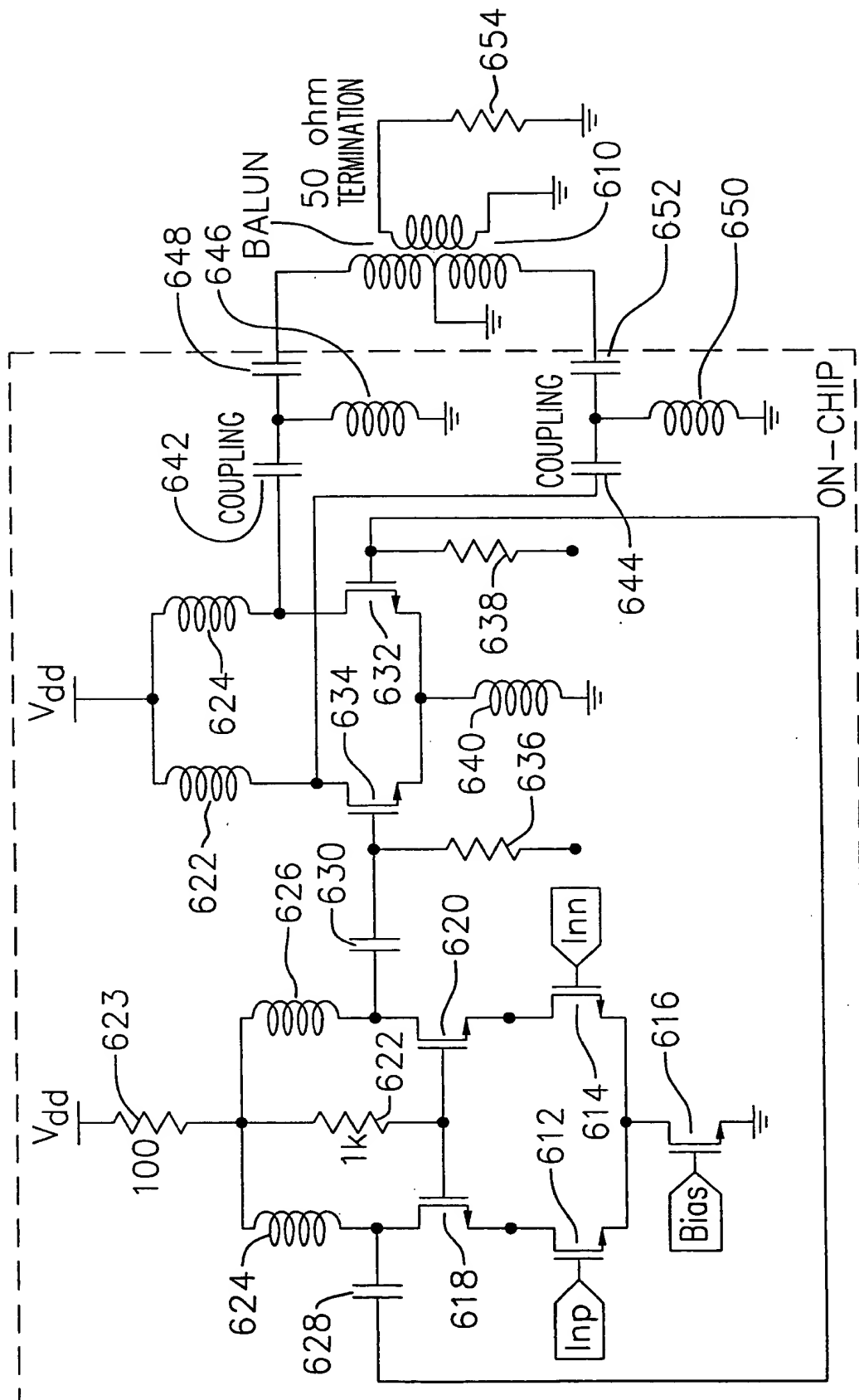


FIG.26a

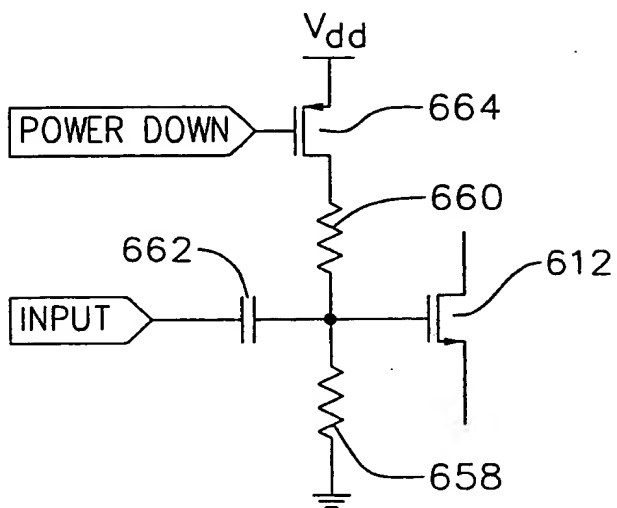


FIG.26b

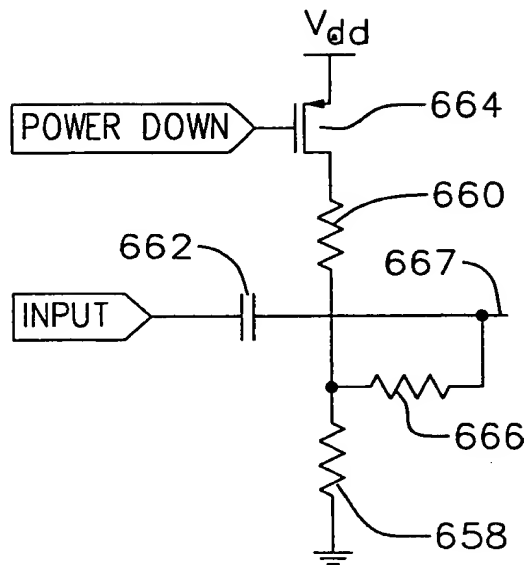


FIG.27

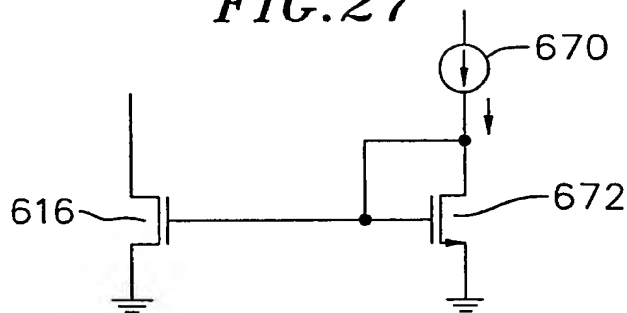
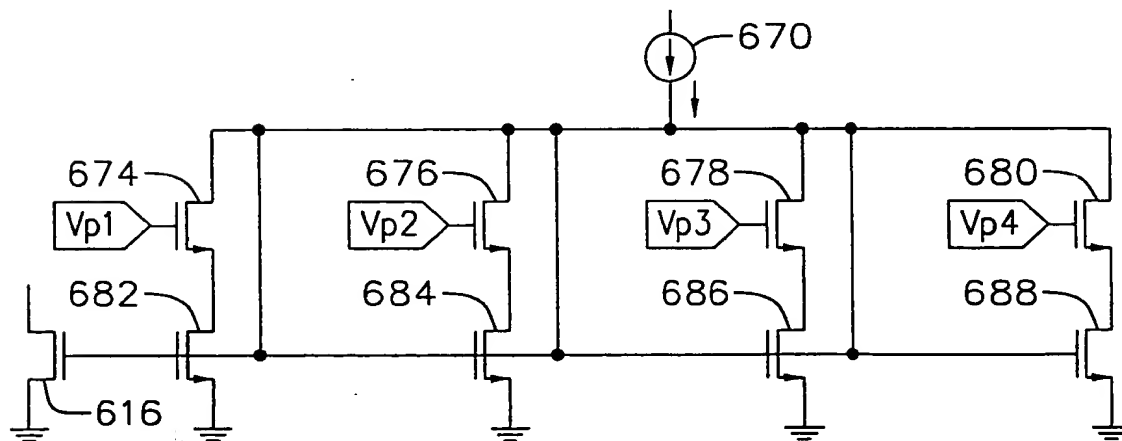


FIG.28



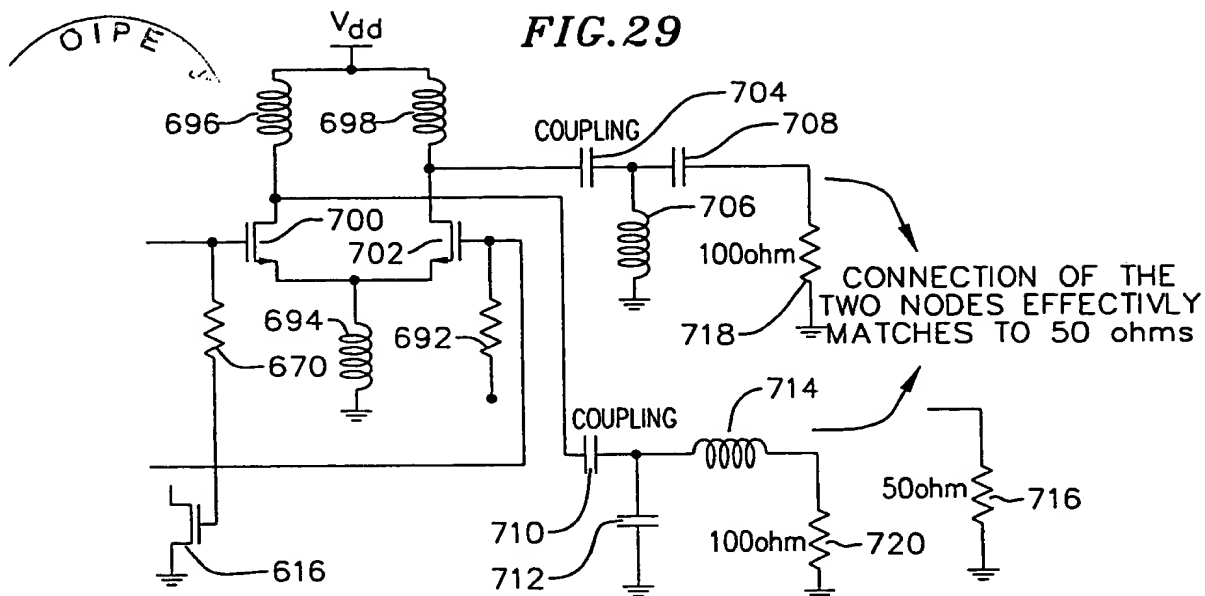
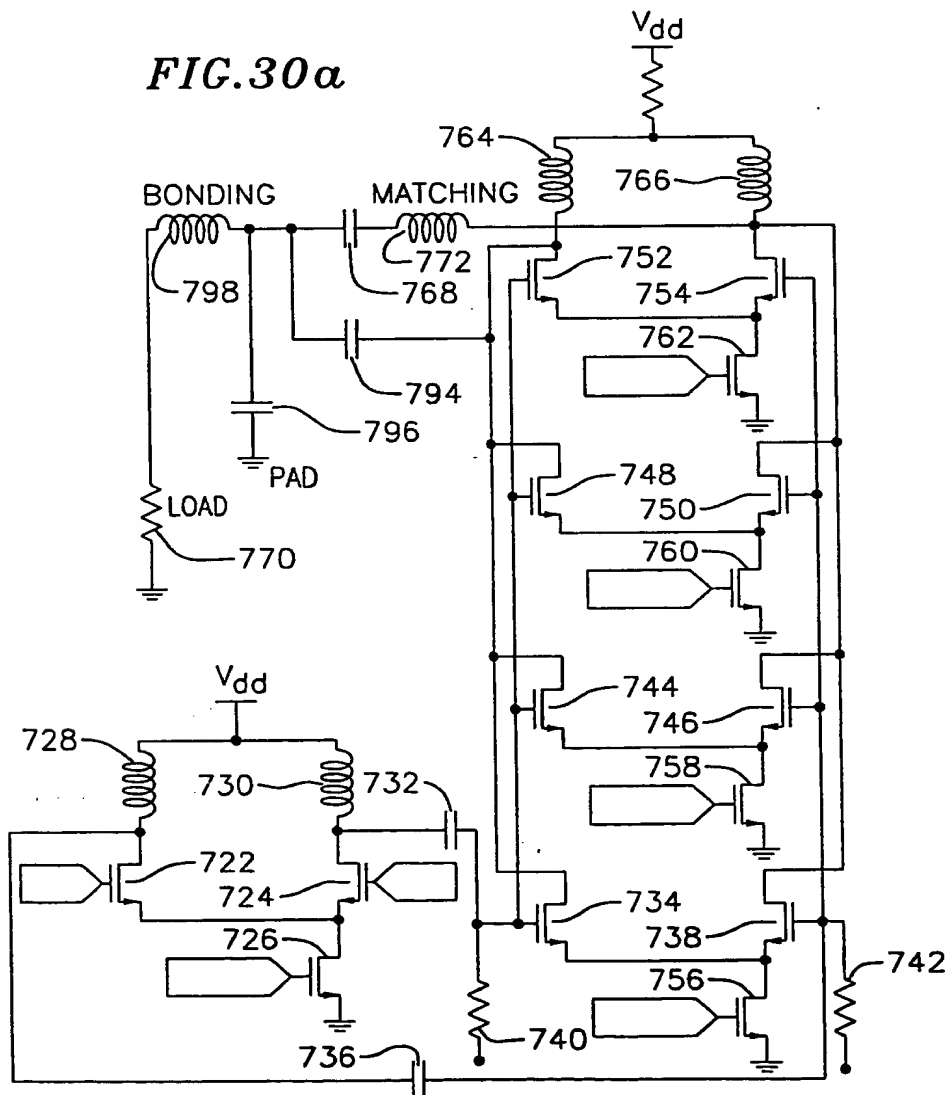


FIG. 30a



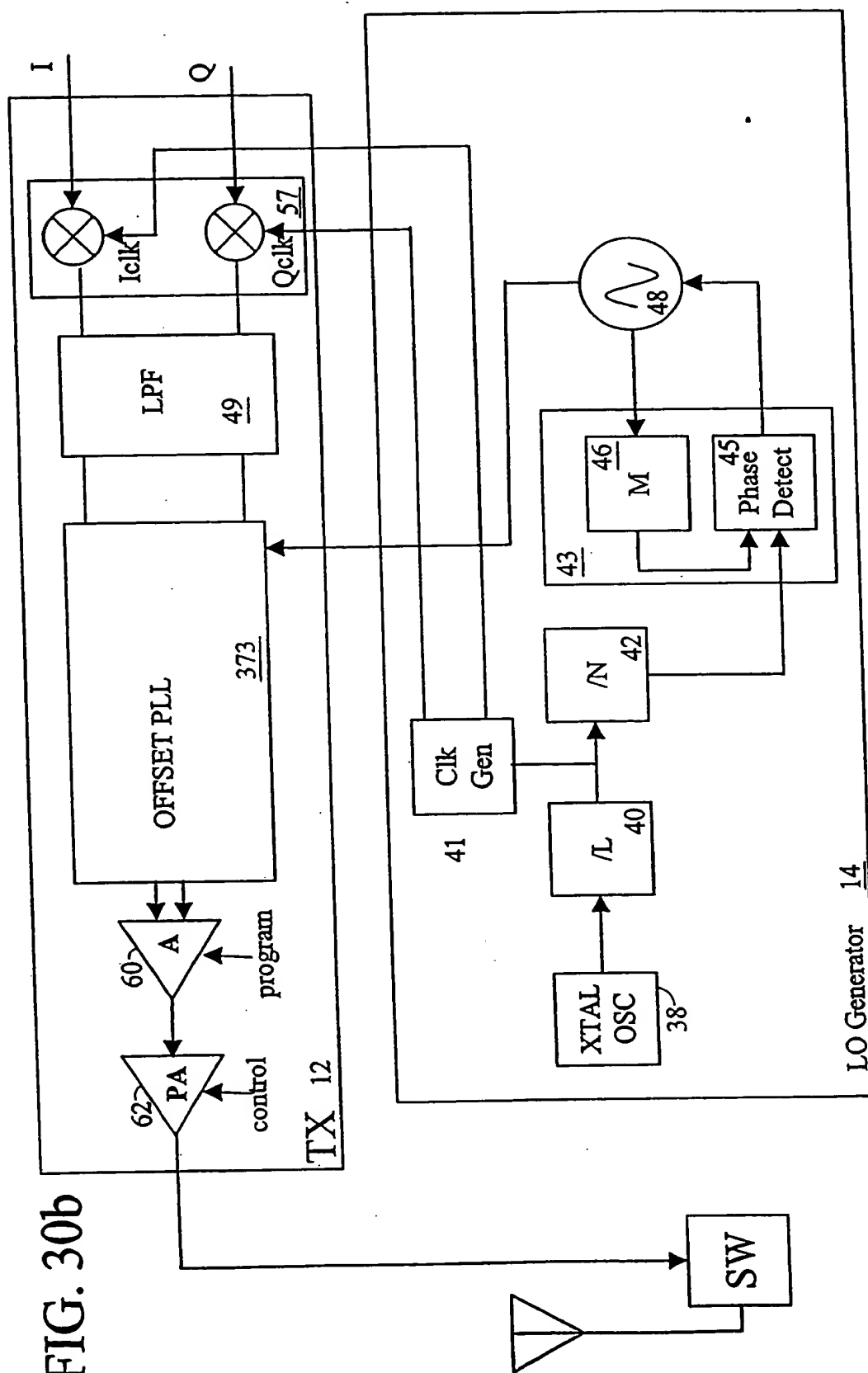
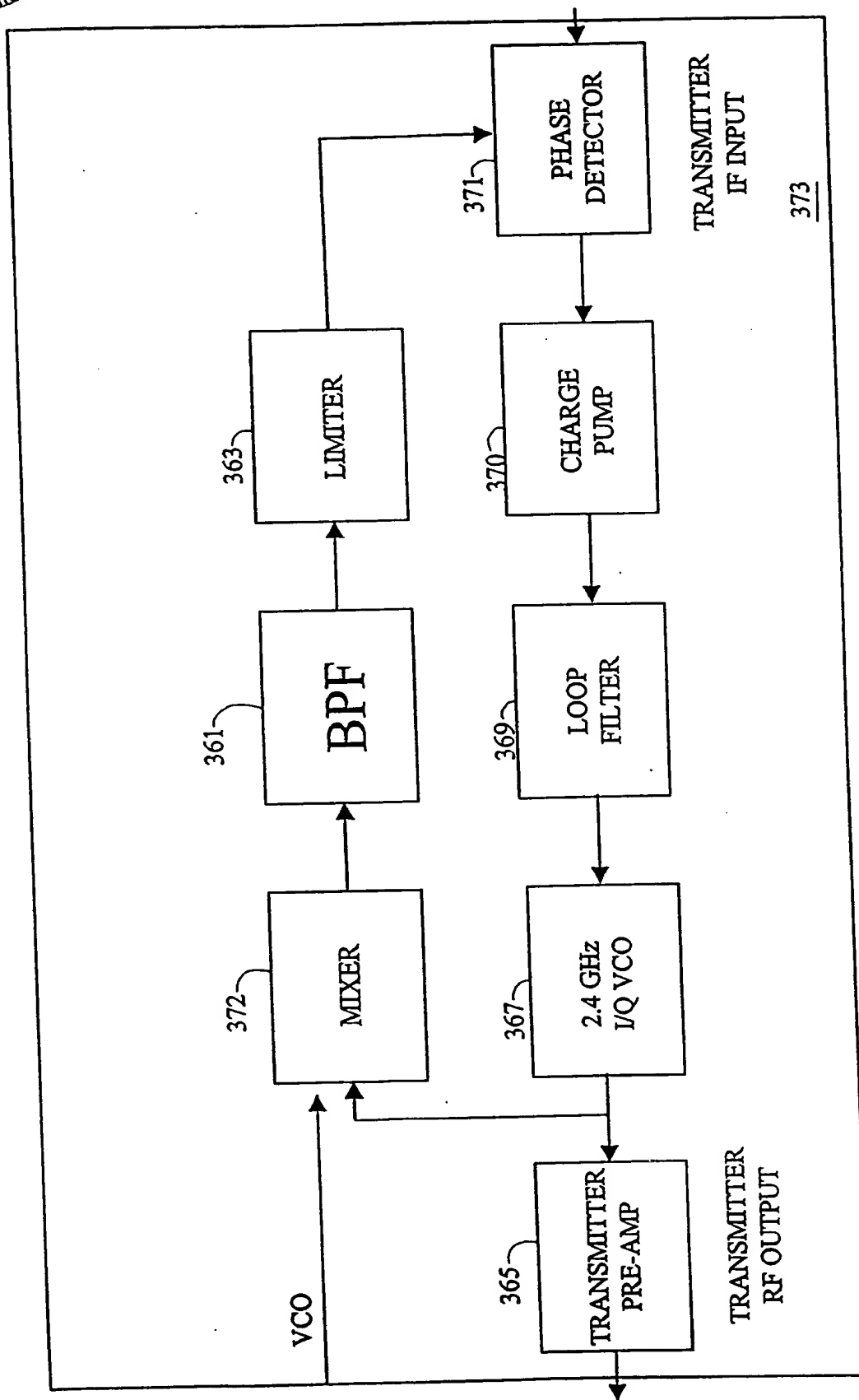


FIG. 30b

FIG. 30c



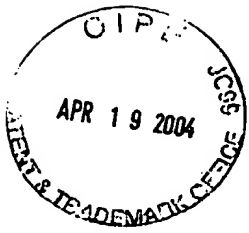


FIG. 30d

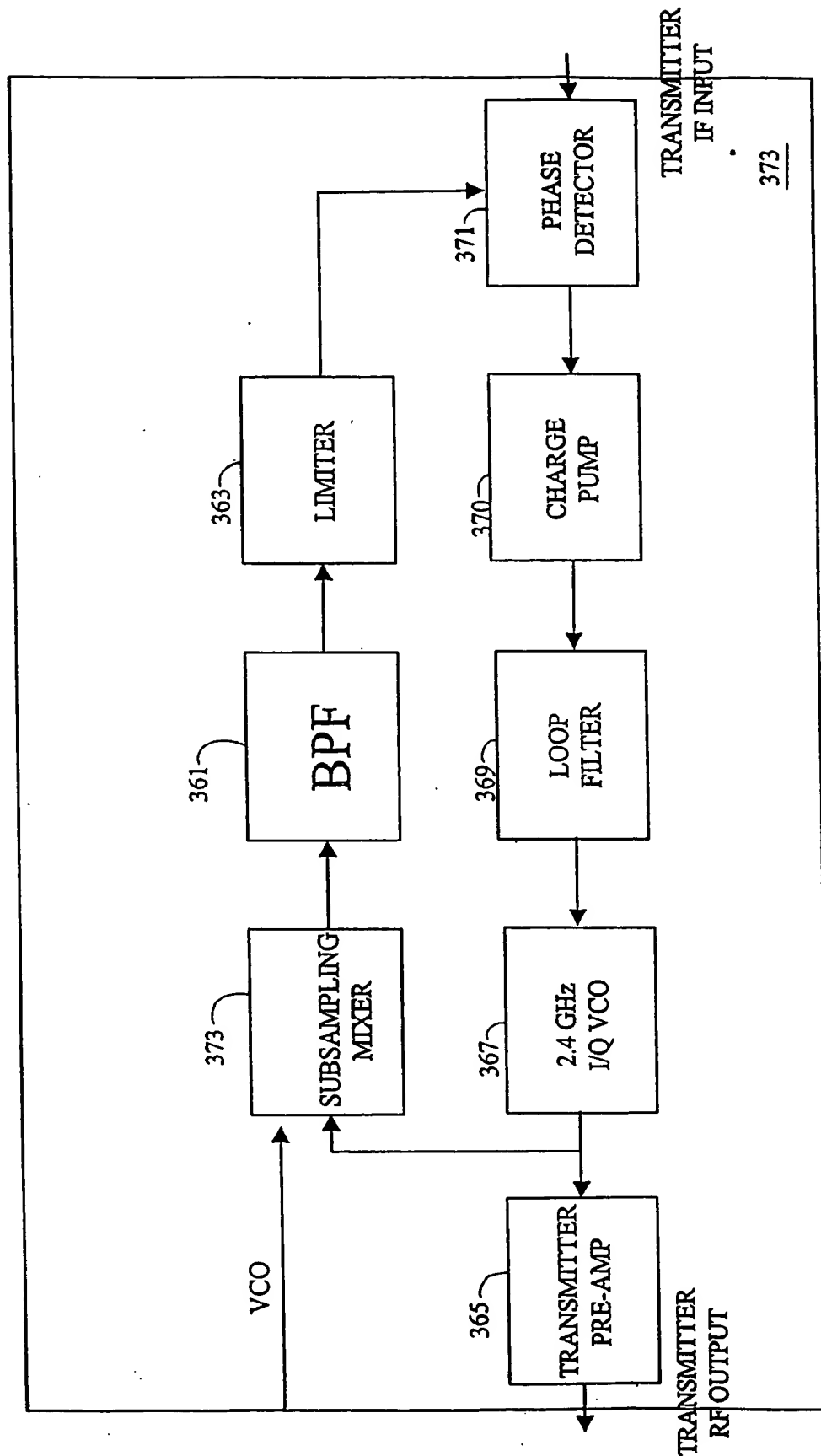
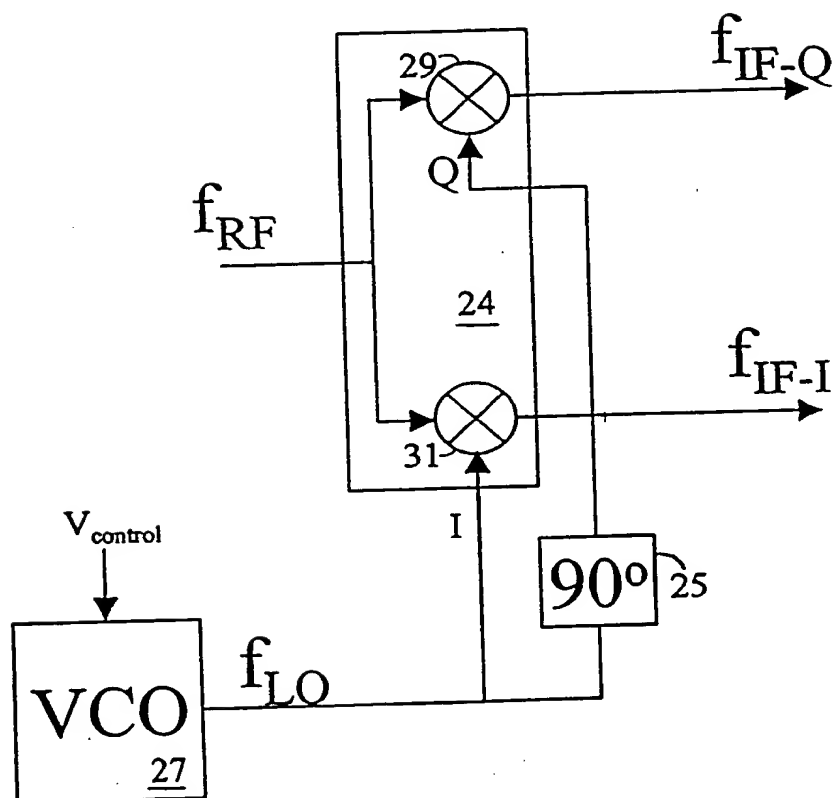
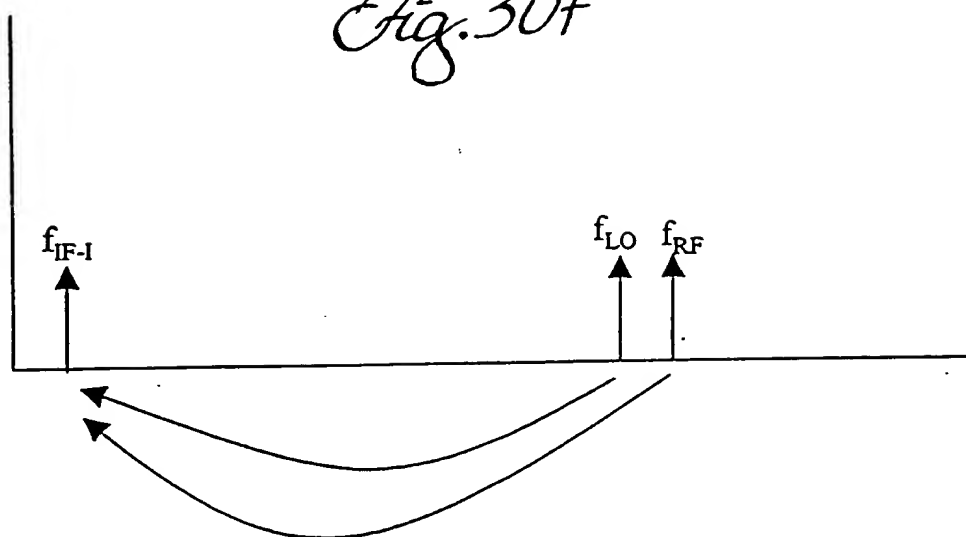
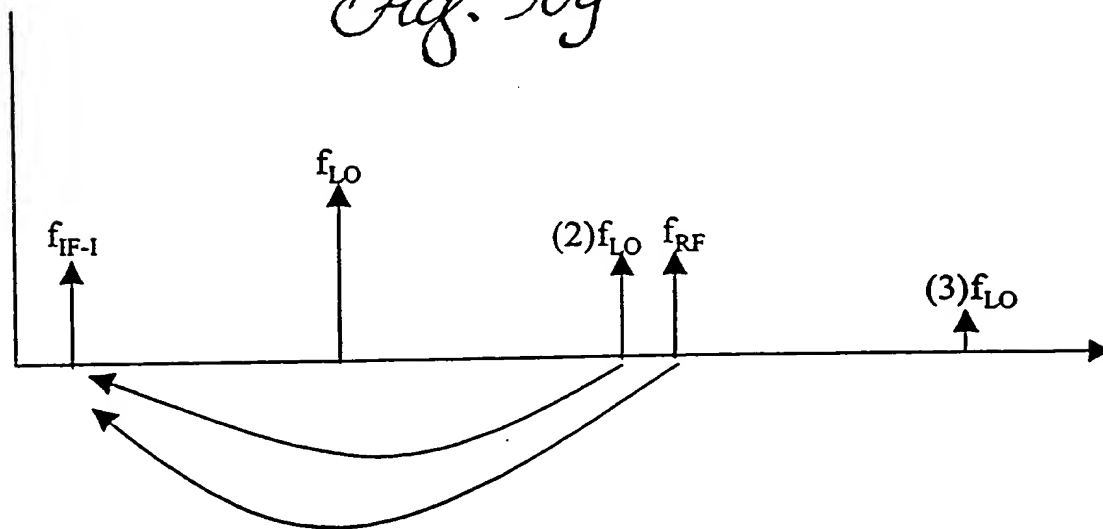


Fig. 30e



*Fig. 30f**Fig. 30g*

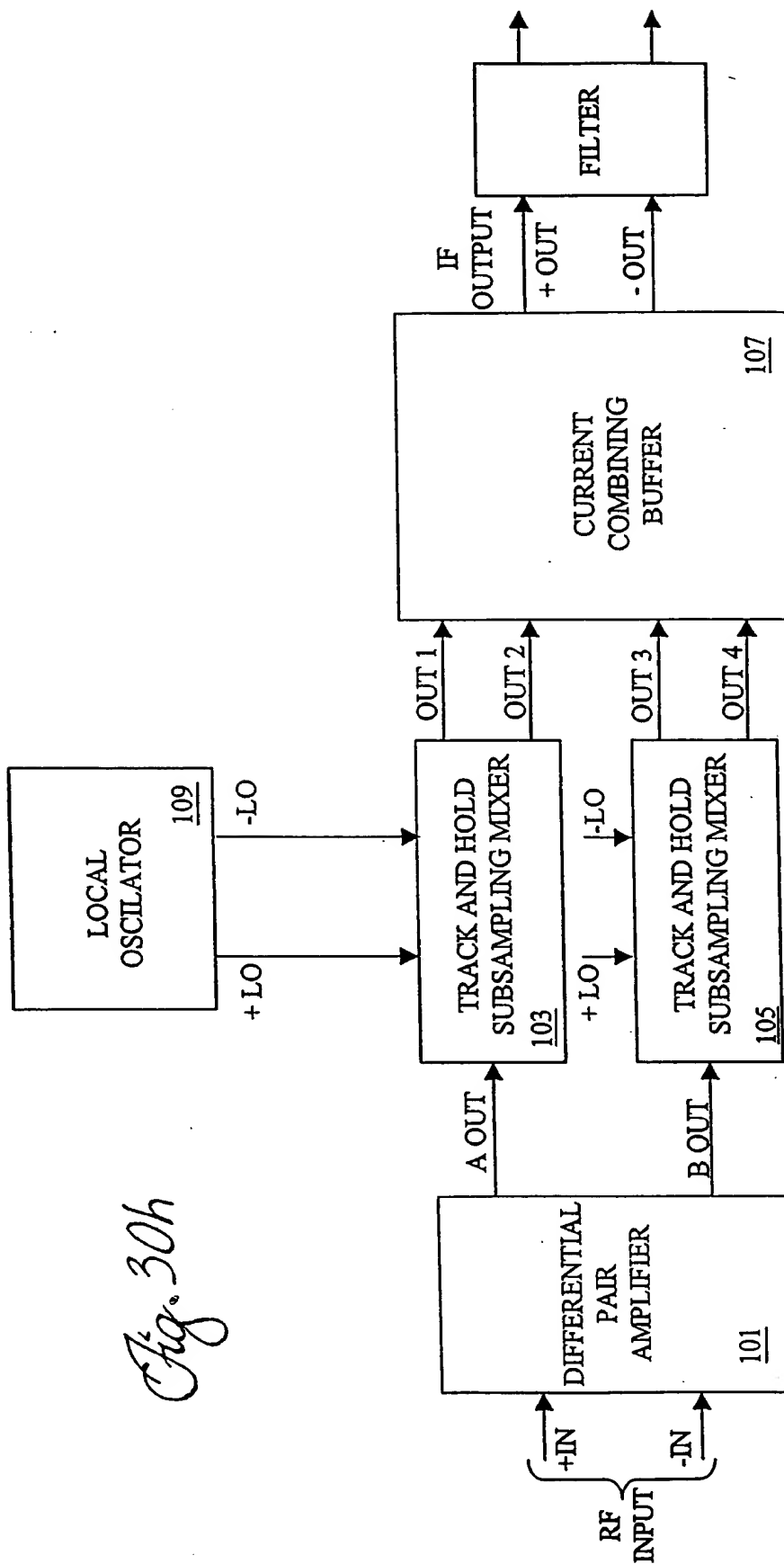
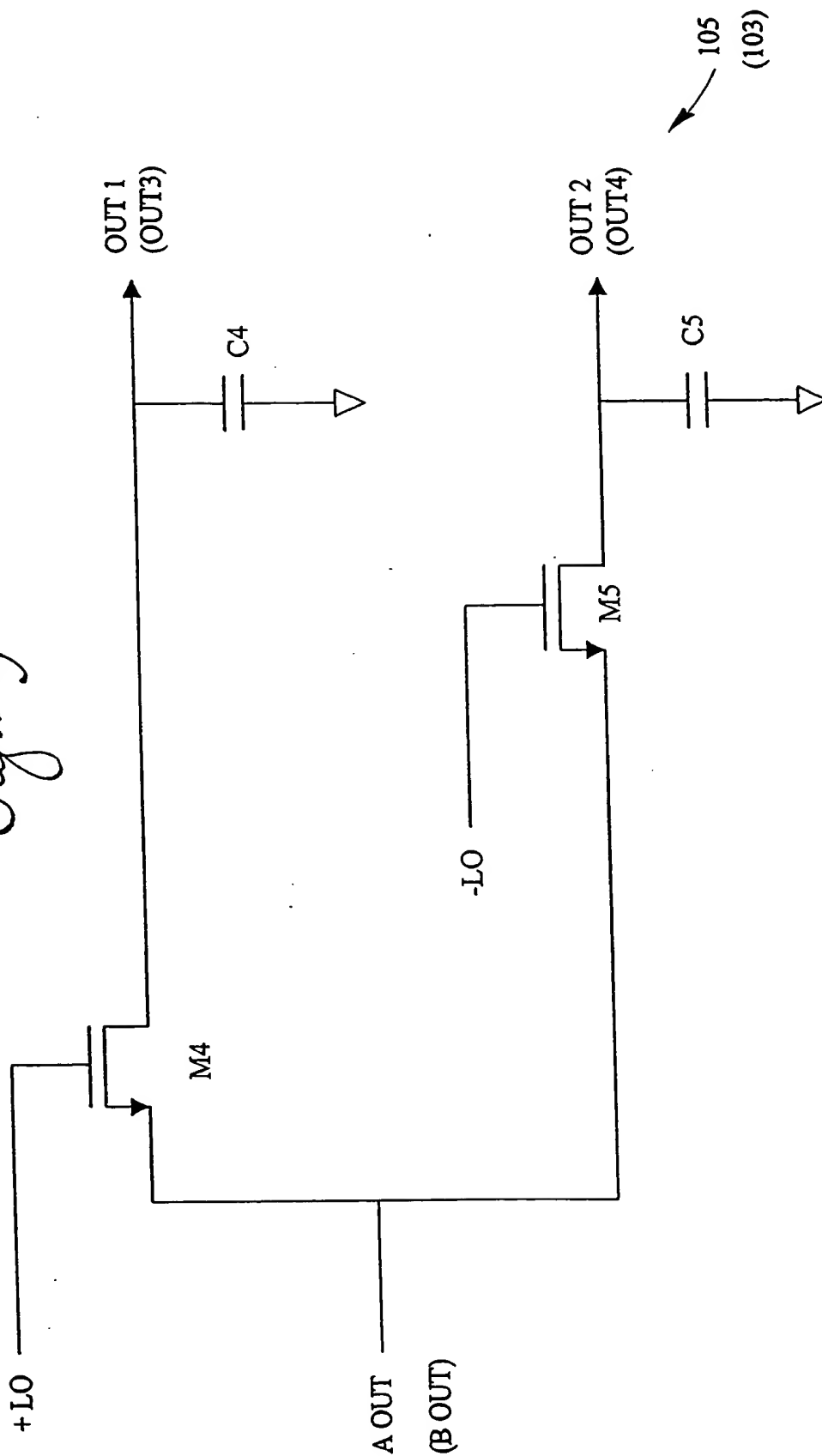


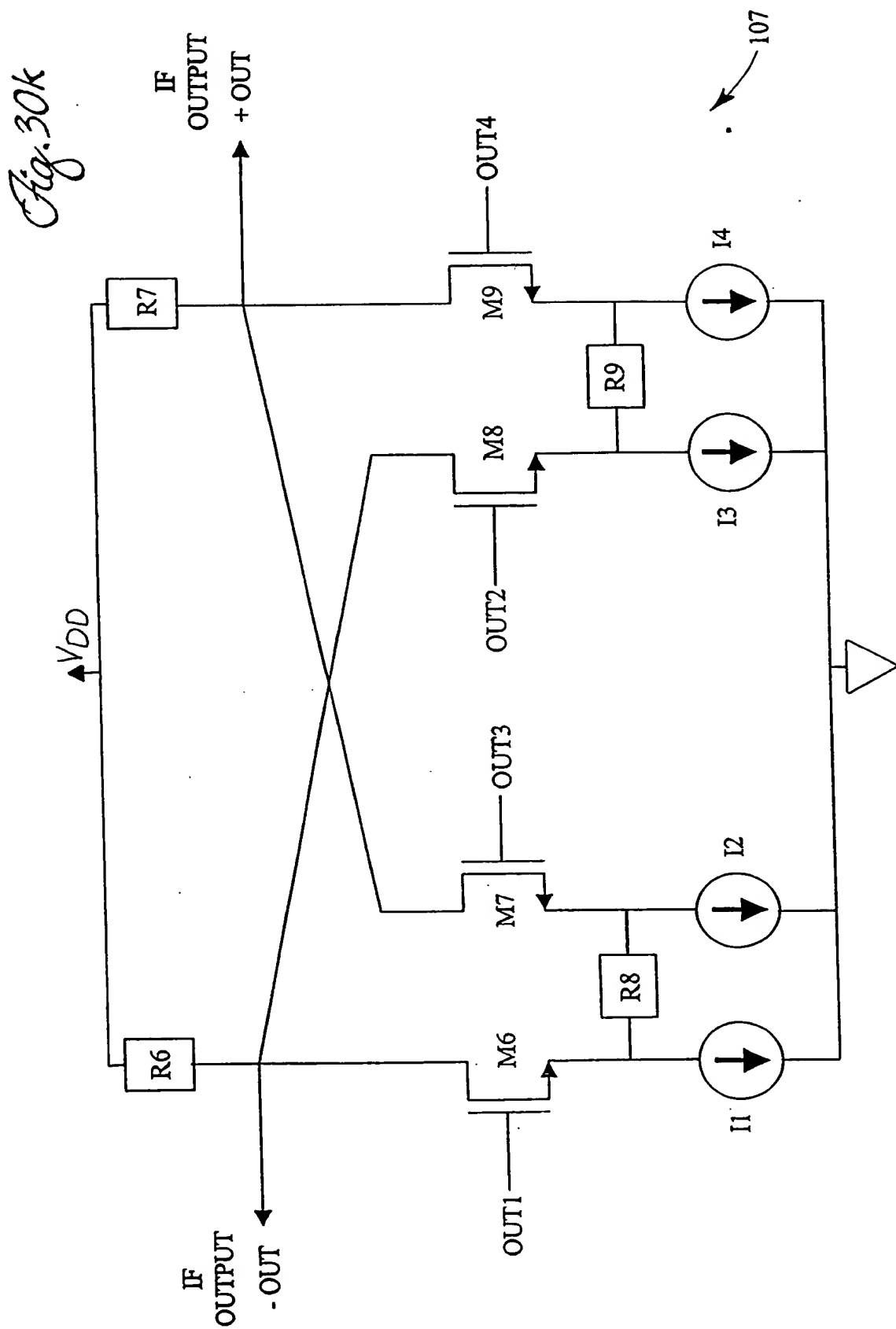
Fig. 30h

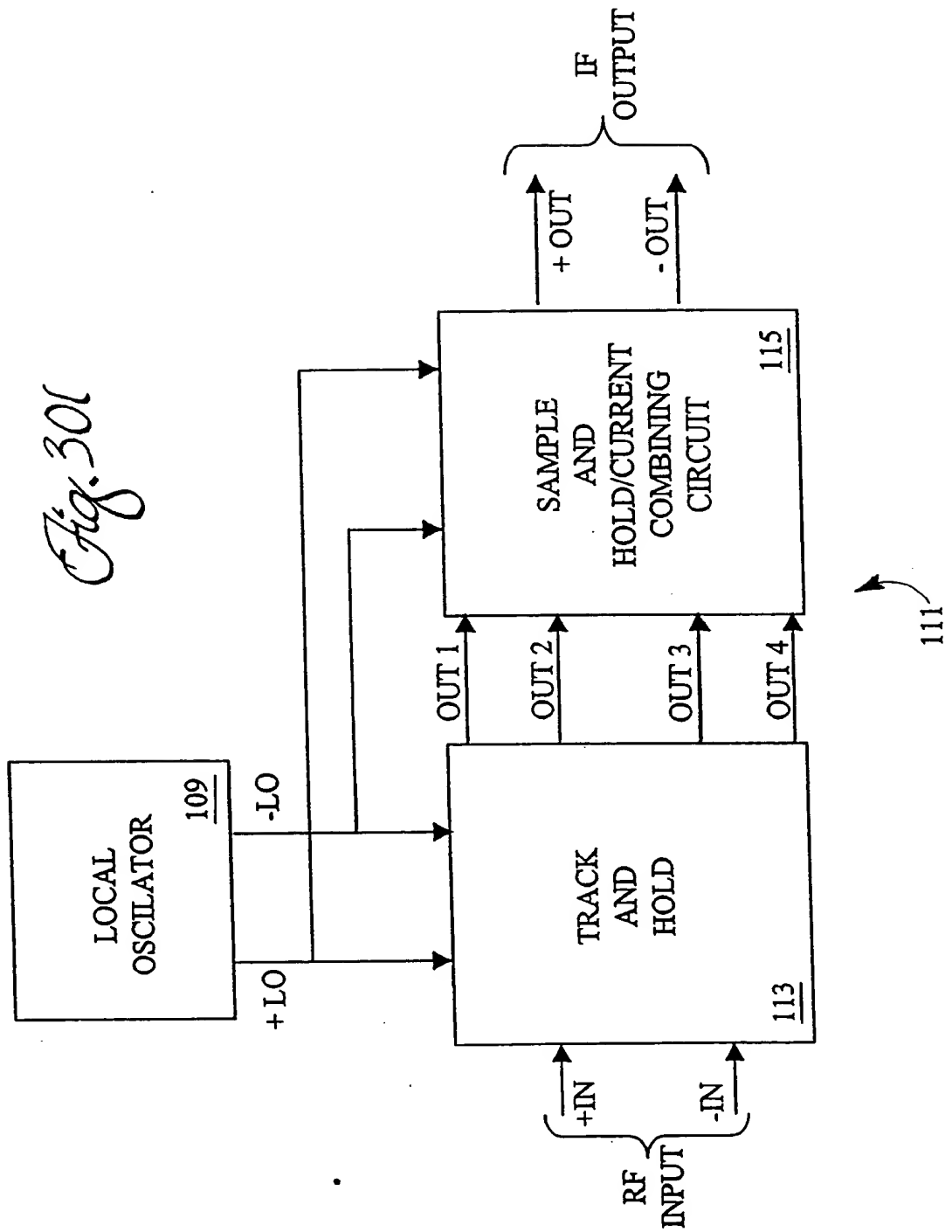
Fig. 30i

The circuit diagram shows a differential amplifier 101. It includes a PMOS load transistor M15 connected to V_{DD} and a differential pair of NMOS transistors M2 and M3. The gates of M2 and M3 are connected to a common input node. The drains of M2 and M3 are connected to a common output node through load inductors L2 and L1, respectively. The output node is connected to a buffer 103. The output of the buffer is labeled B OUT. The input to the buffer is labeled +IN. The output of the differential pair is labeled A OUT. The circuit is labeled 101.

Fig. 30j







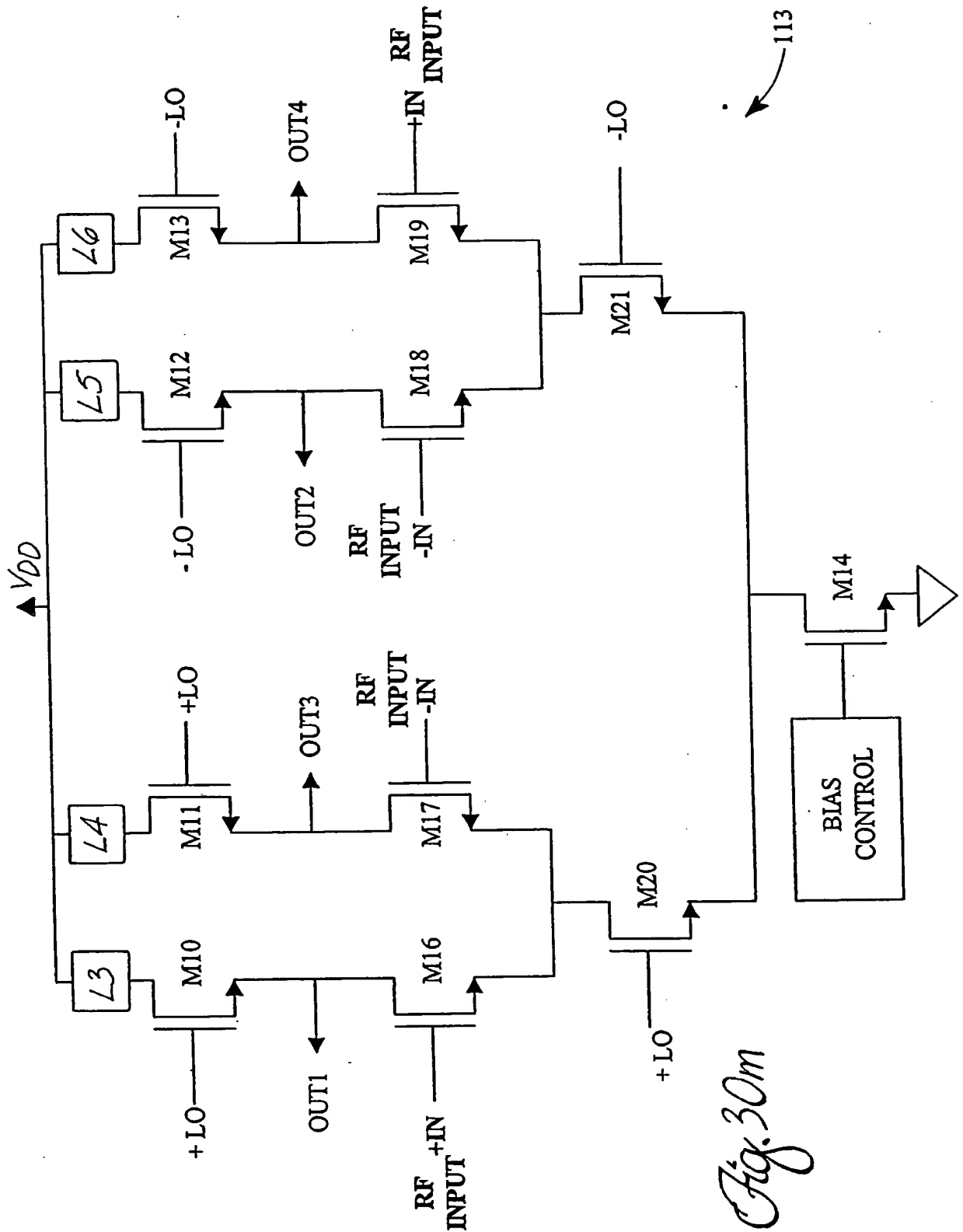


Fig. 30m

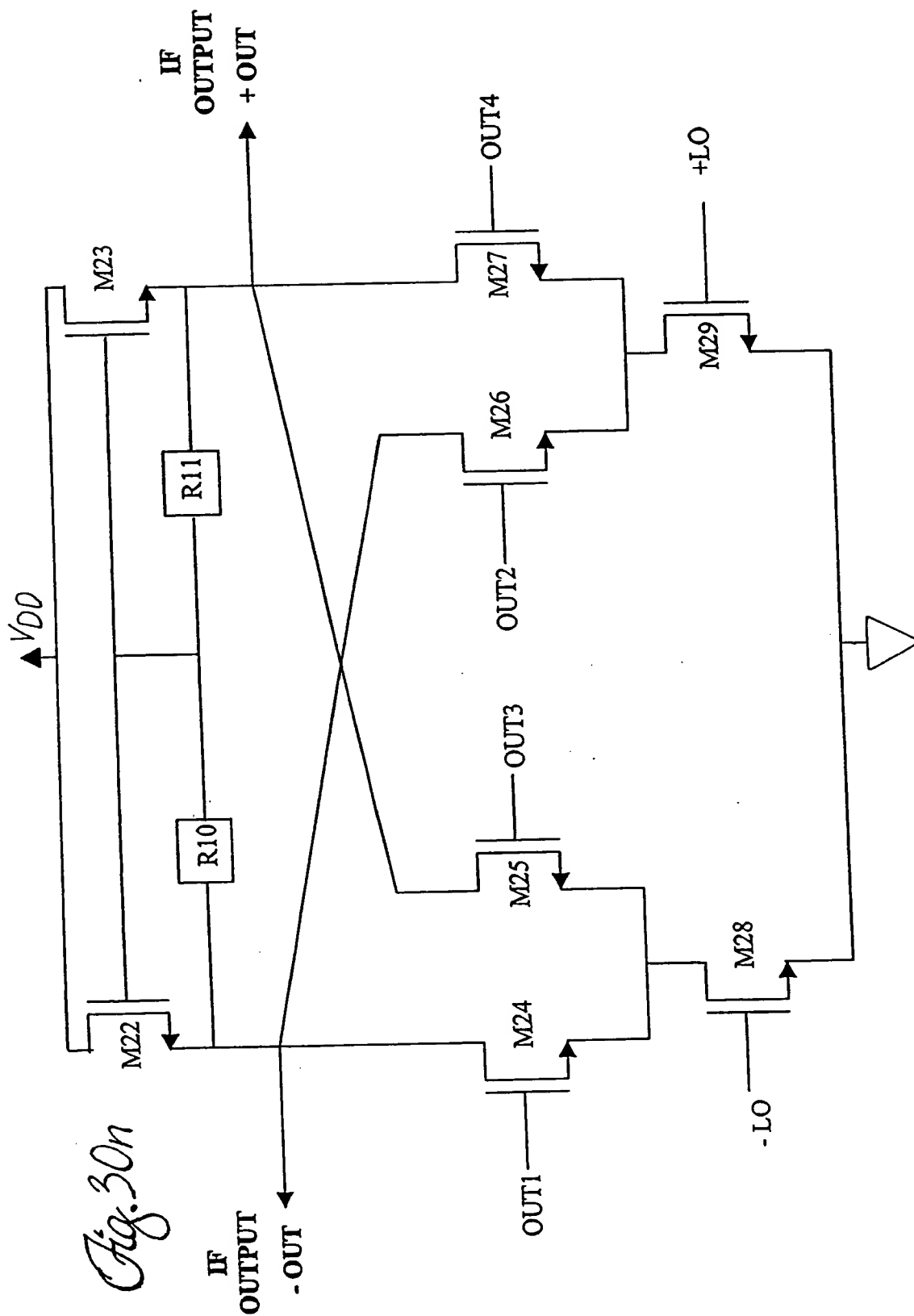


Fig. 30n

FIG. 31a

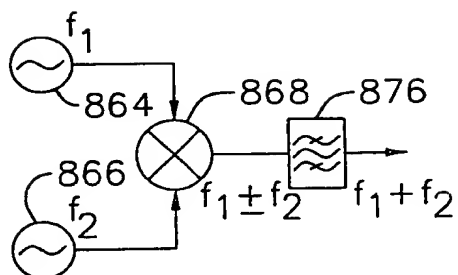


FIG. 31b

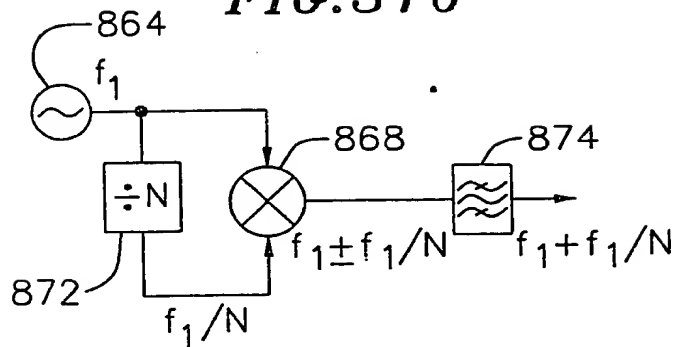


FIG. 32

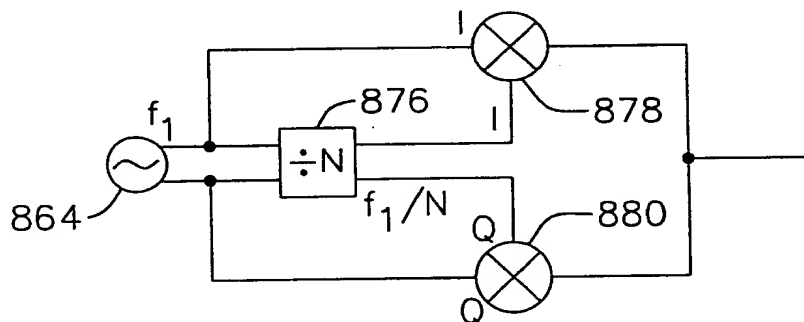


FIG. 33

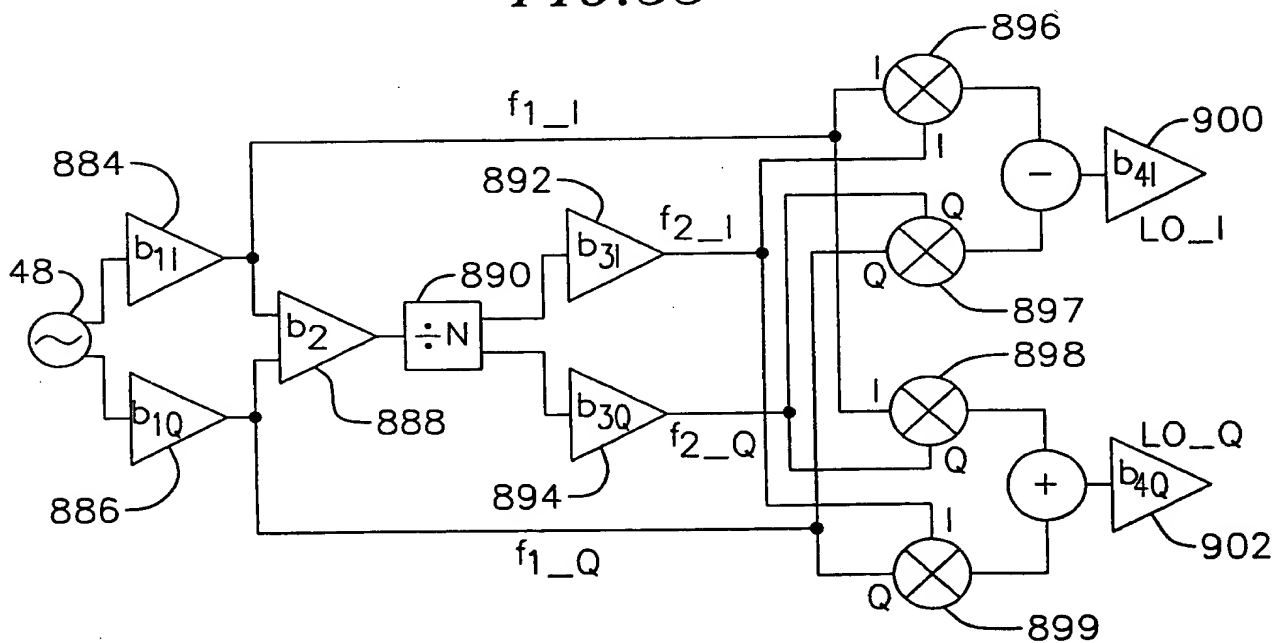


FIG. 33b

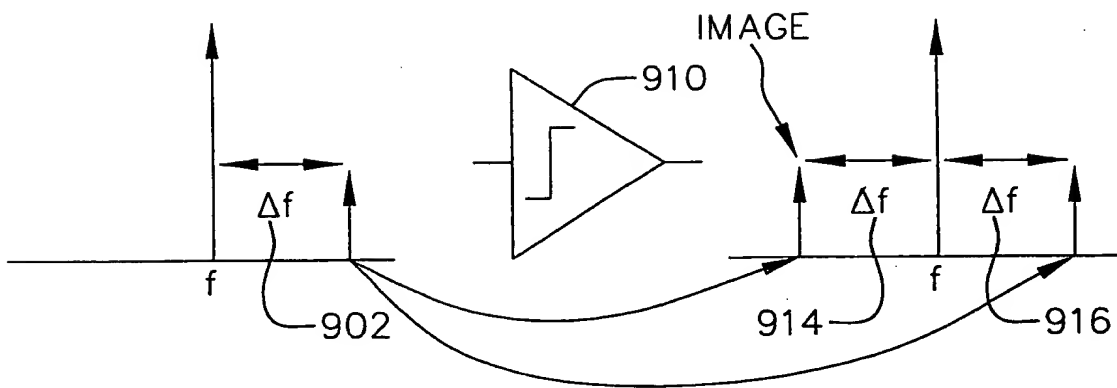


FIG. 34

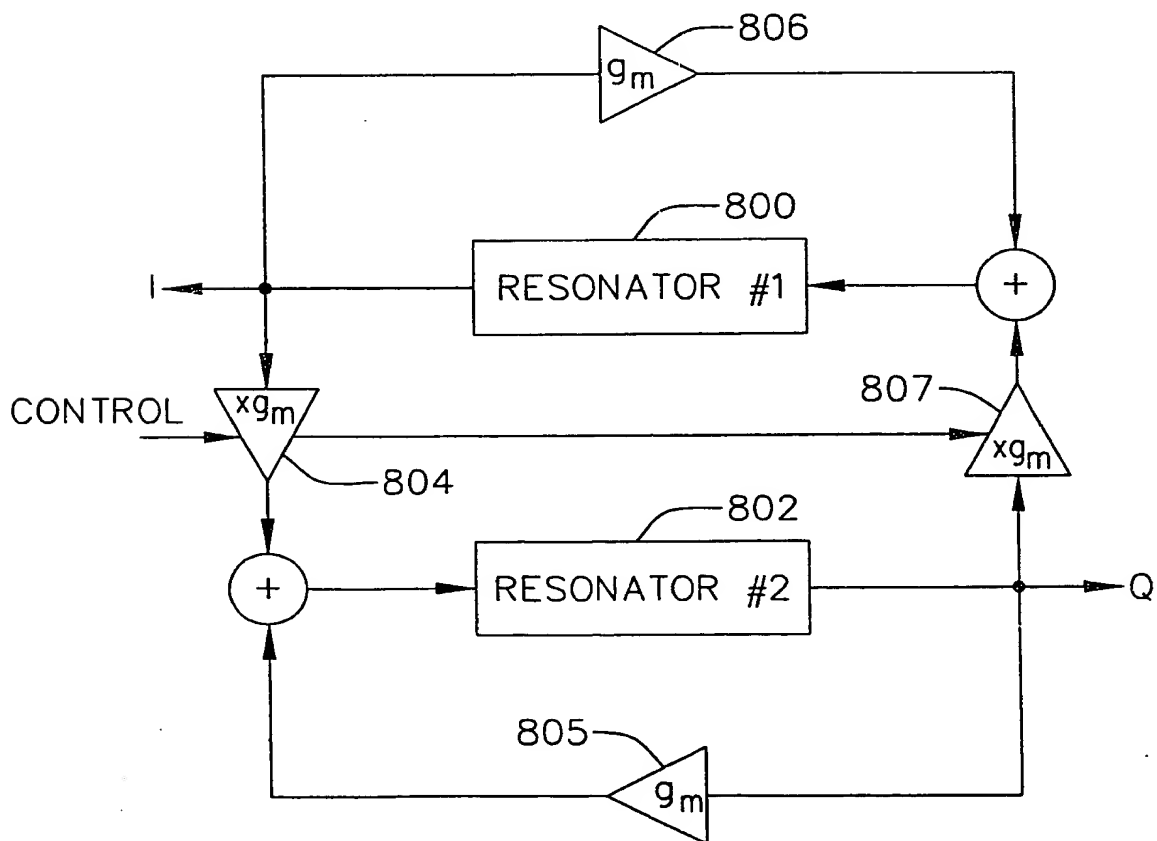
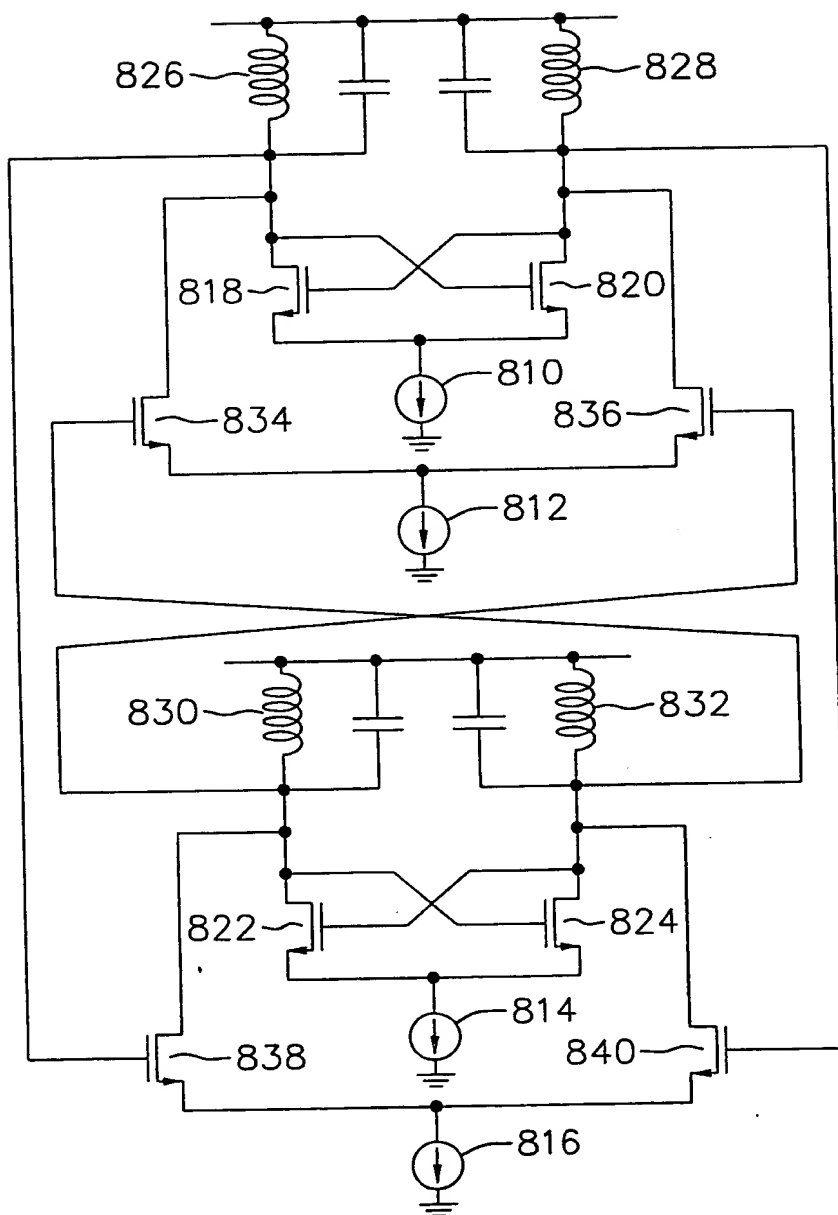
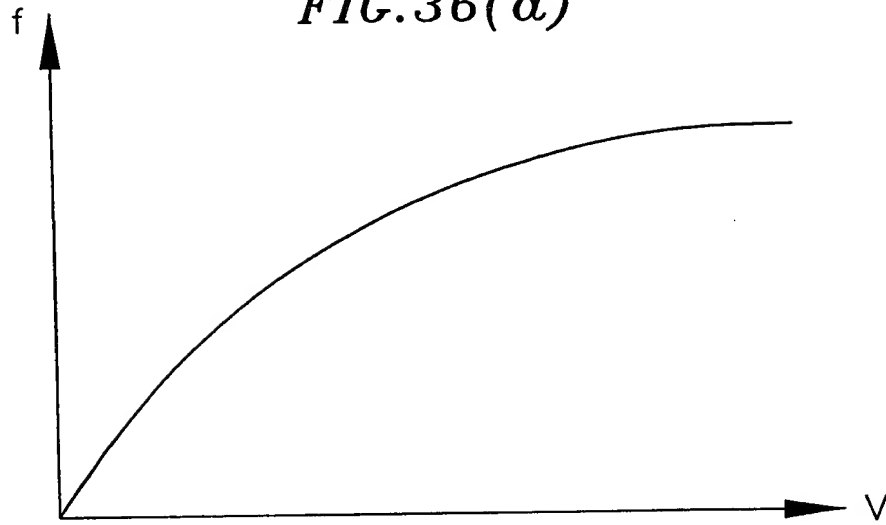
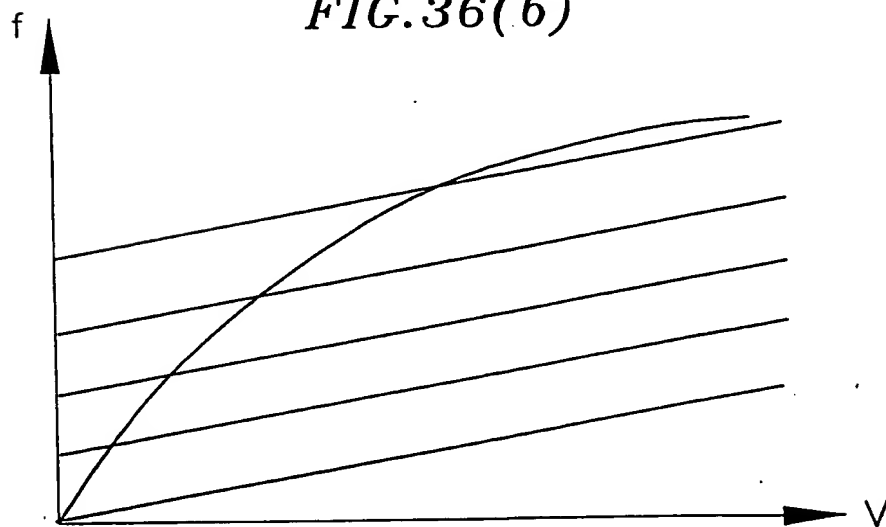


FIG. 35



*FIG.36(a)*

TYPICAL VCO TUNING CURVE

FIG.36(b)

SEGMENTED VCO TUNING CURVE

FIG. 37a

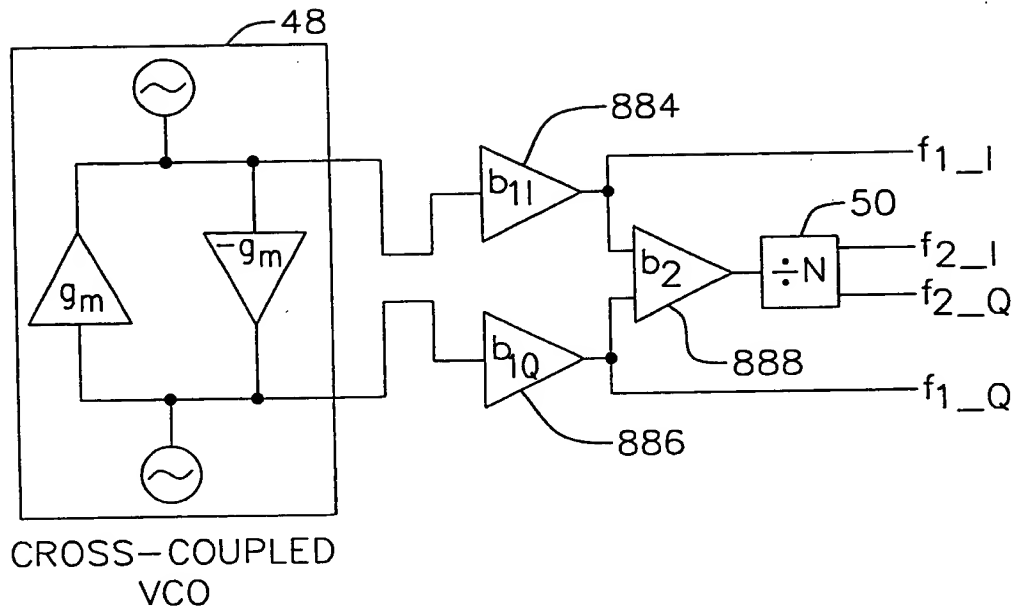
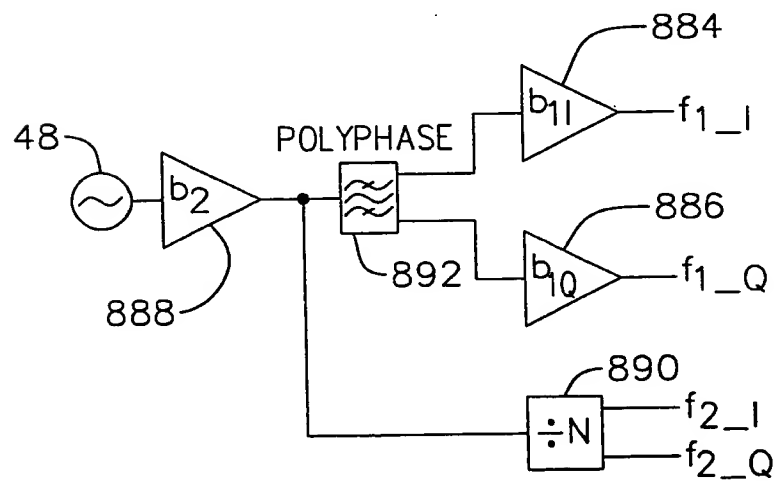
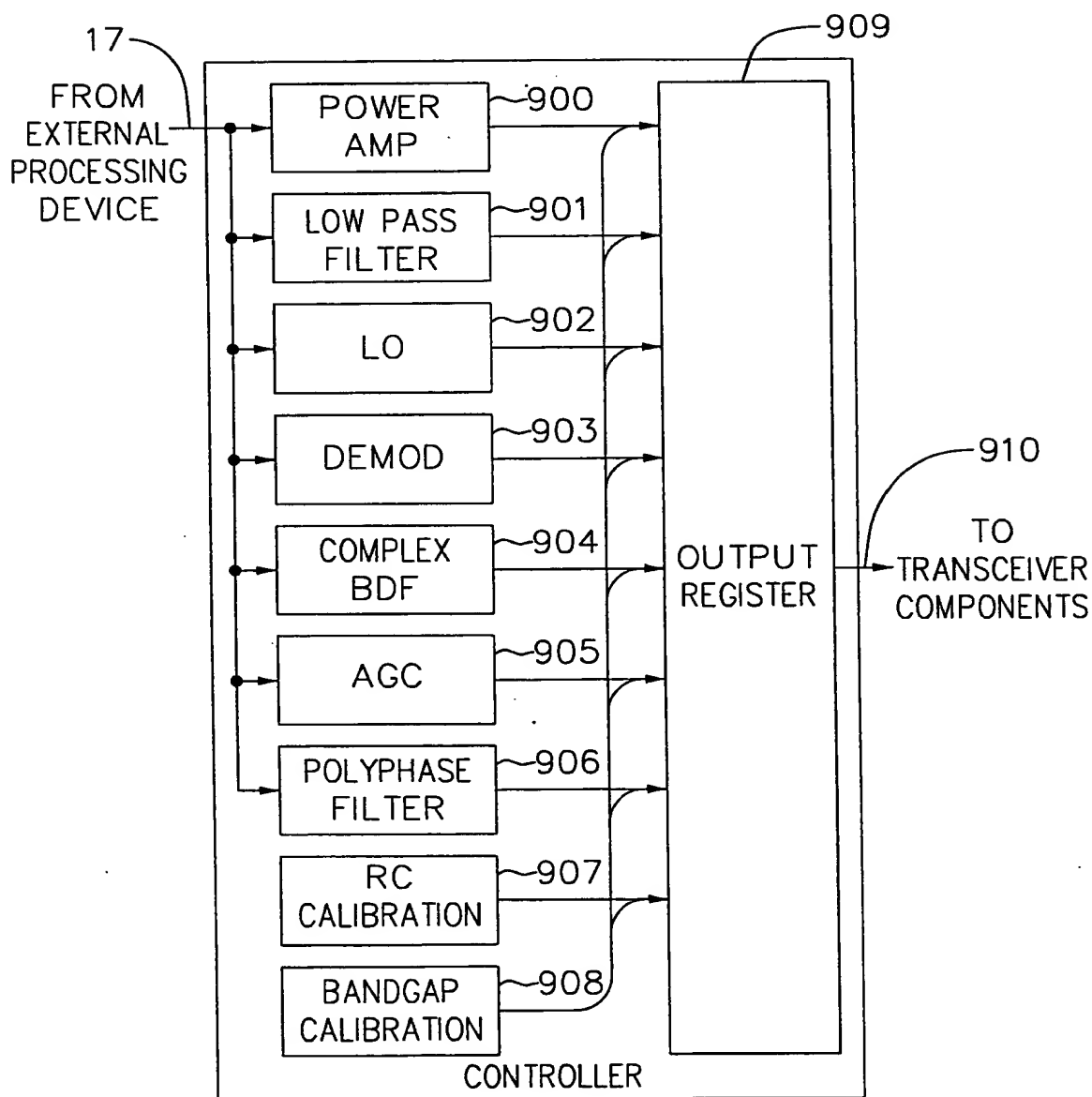
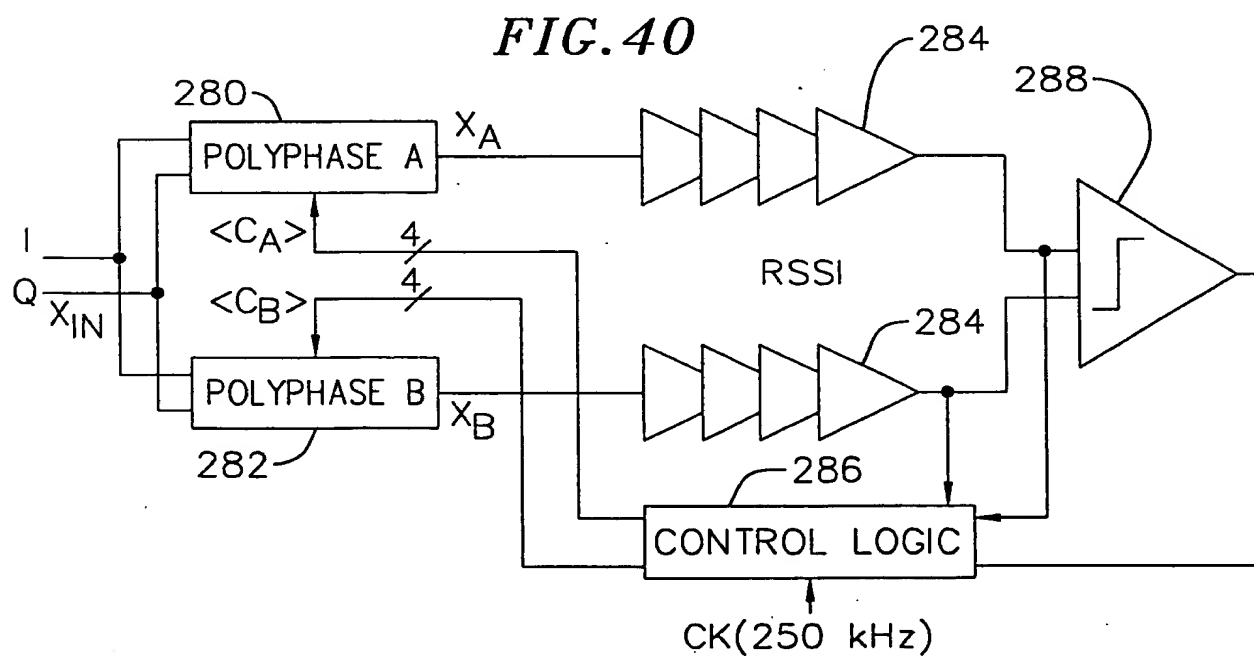
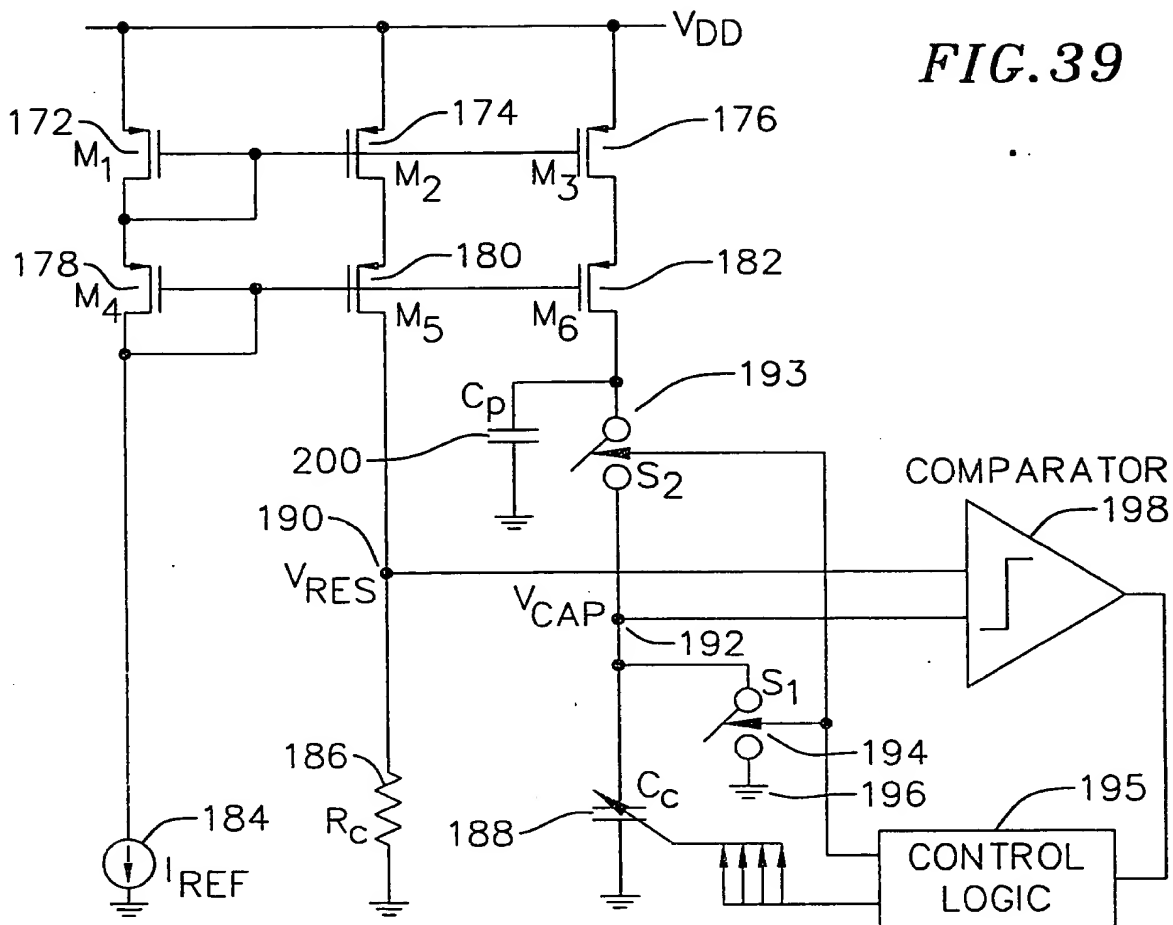


FIG. 37b



*FIG.38*



OIPE

FIG. 41

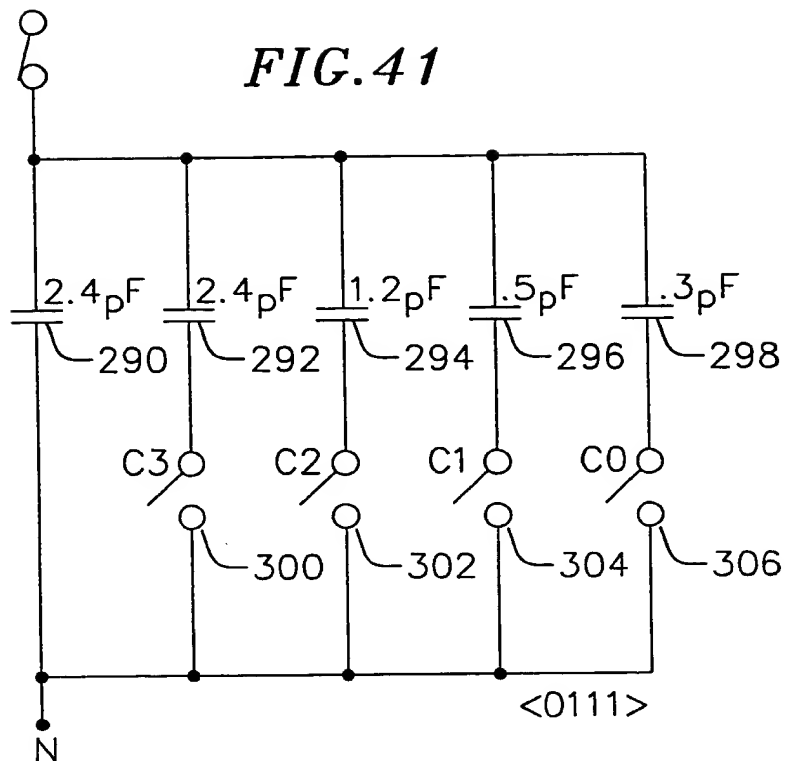


FIG. 42

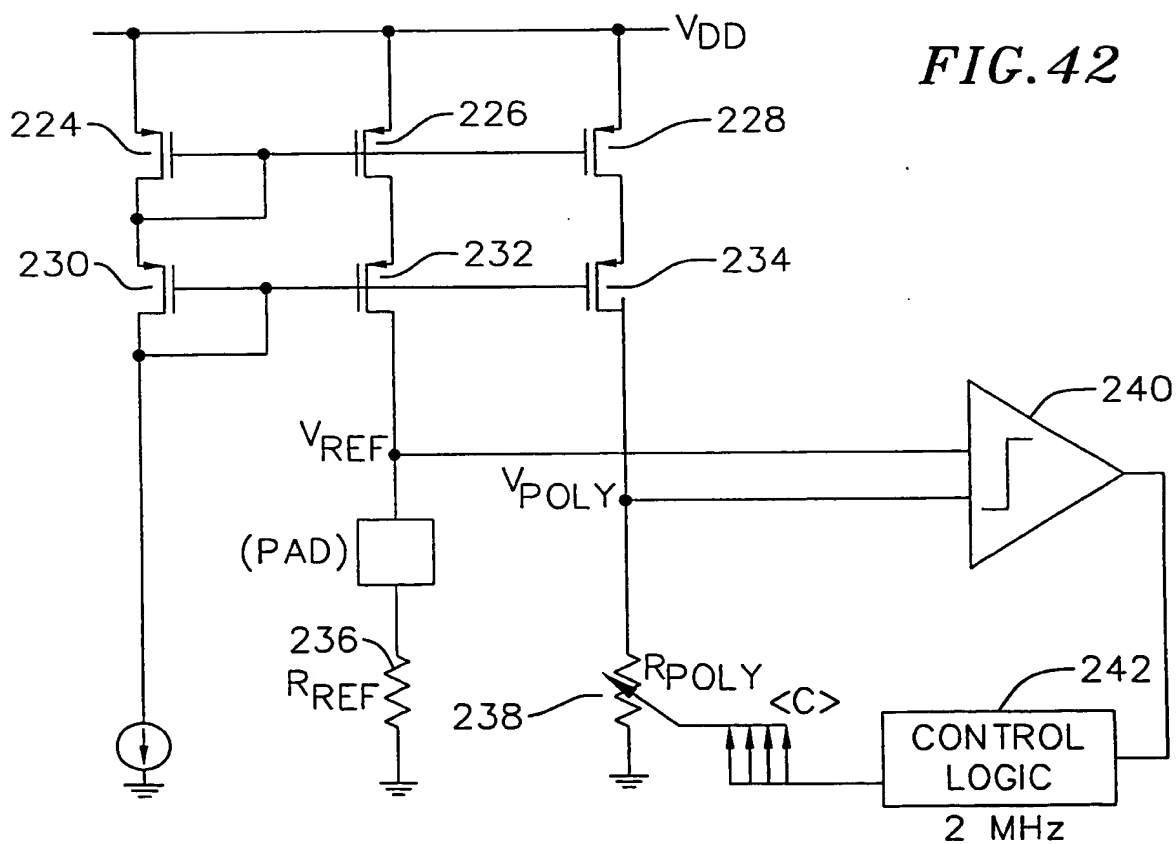


FIG. 43

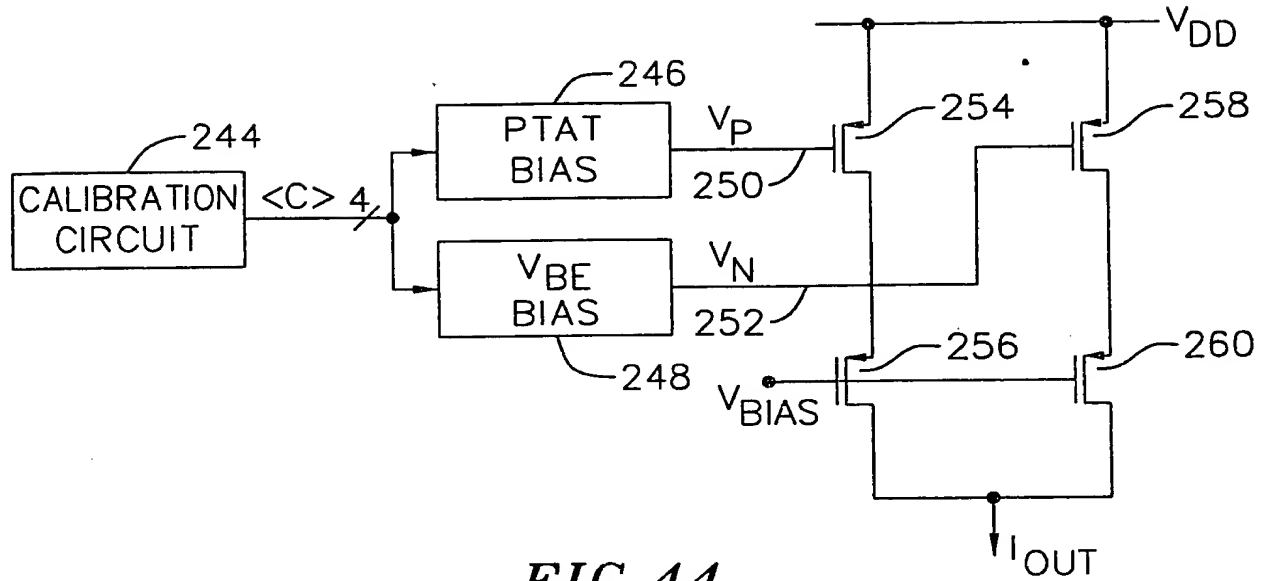


FIG. 44

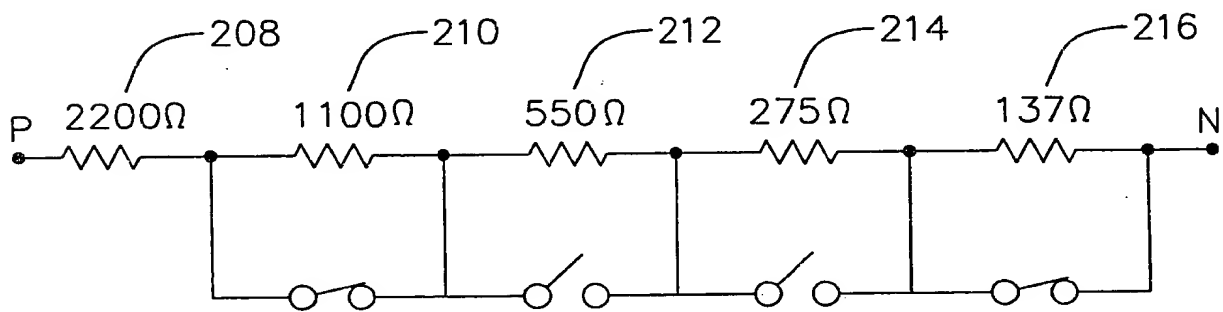
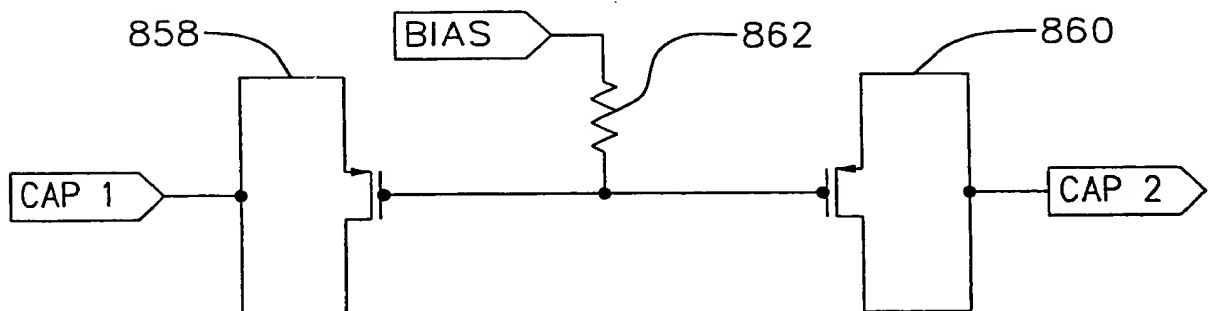


FIG. 45



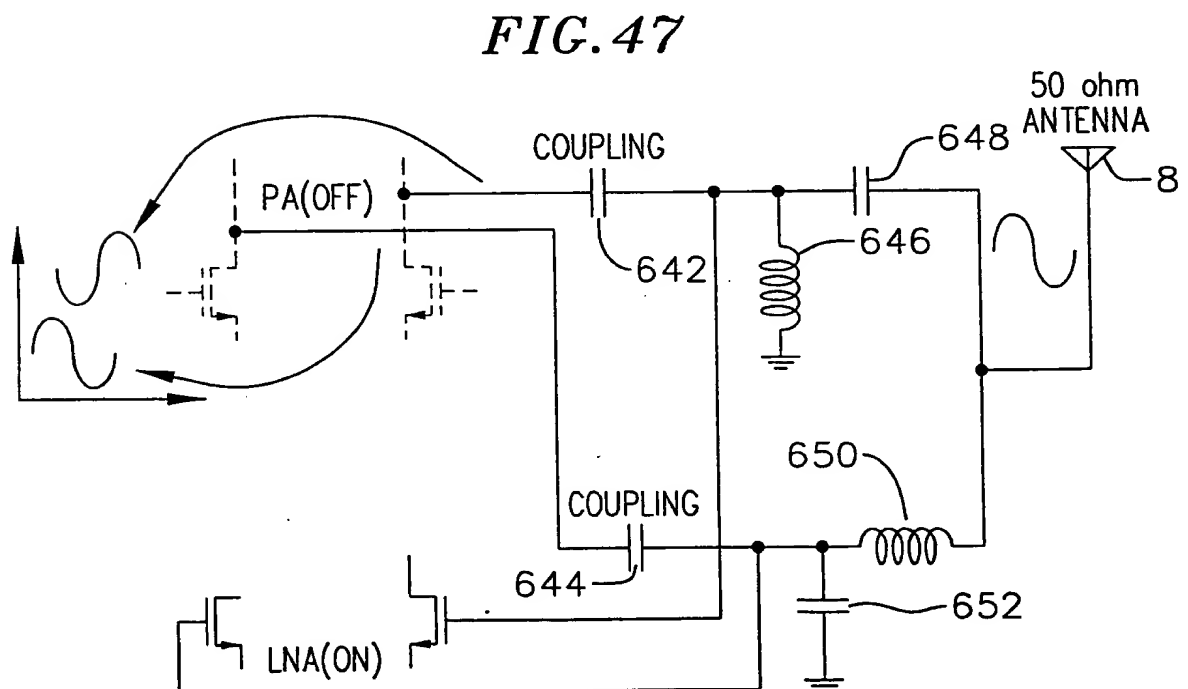
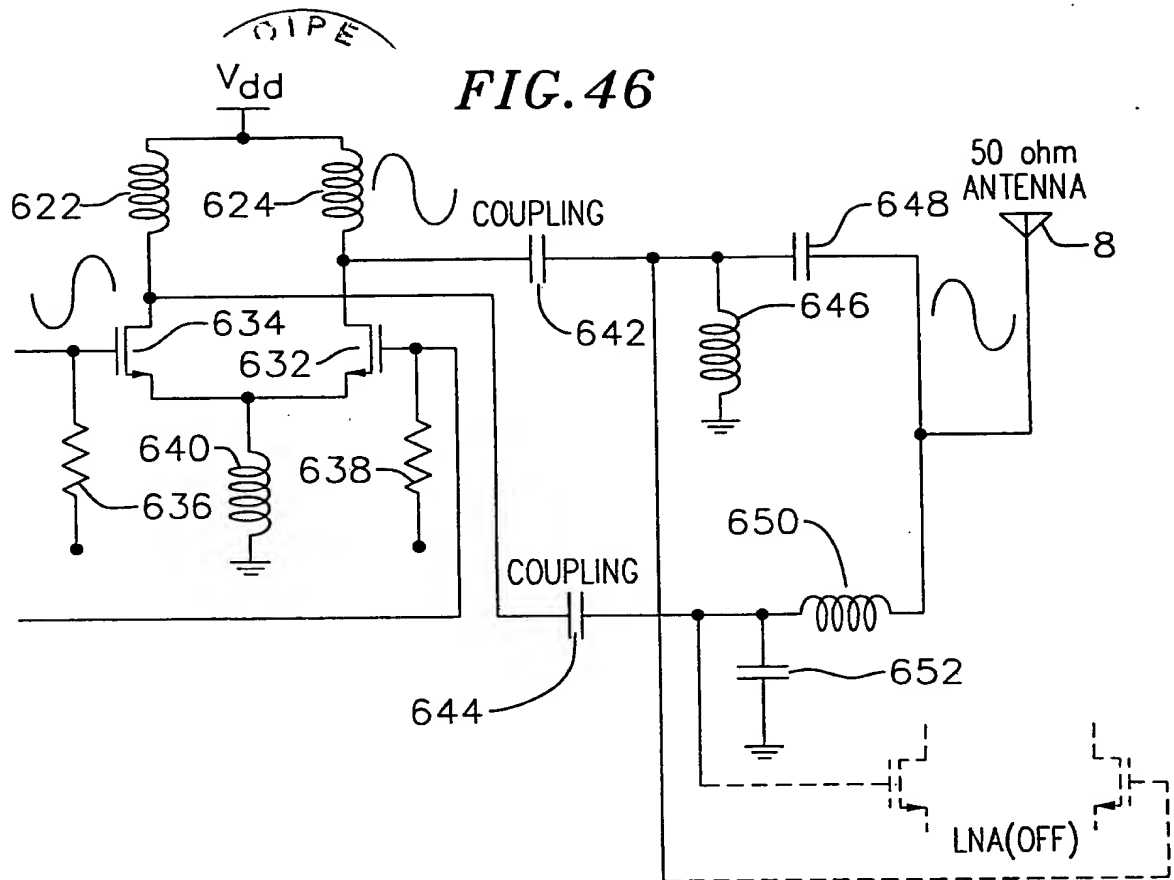
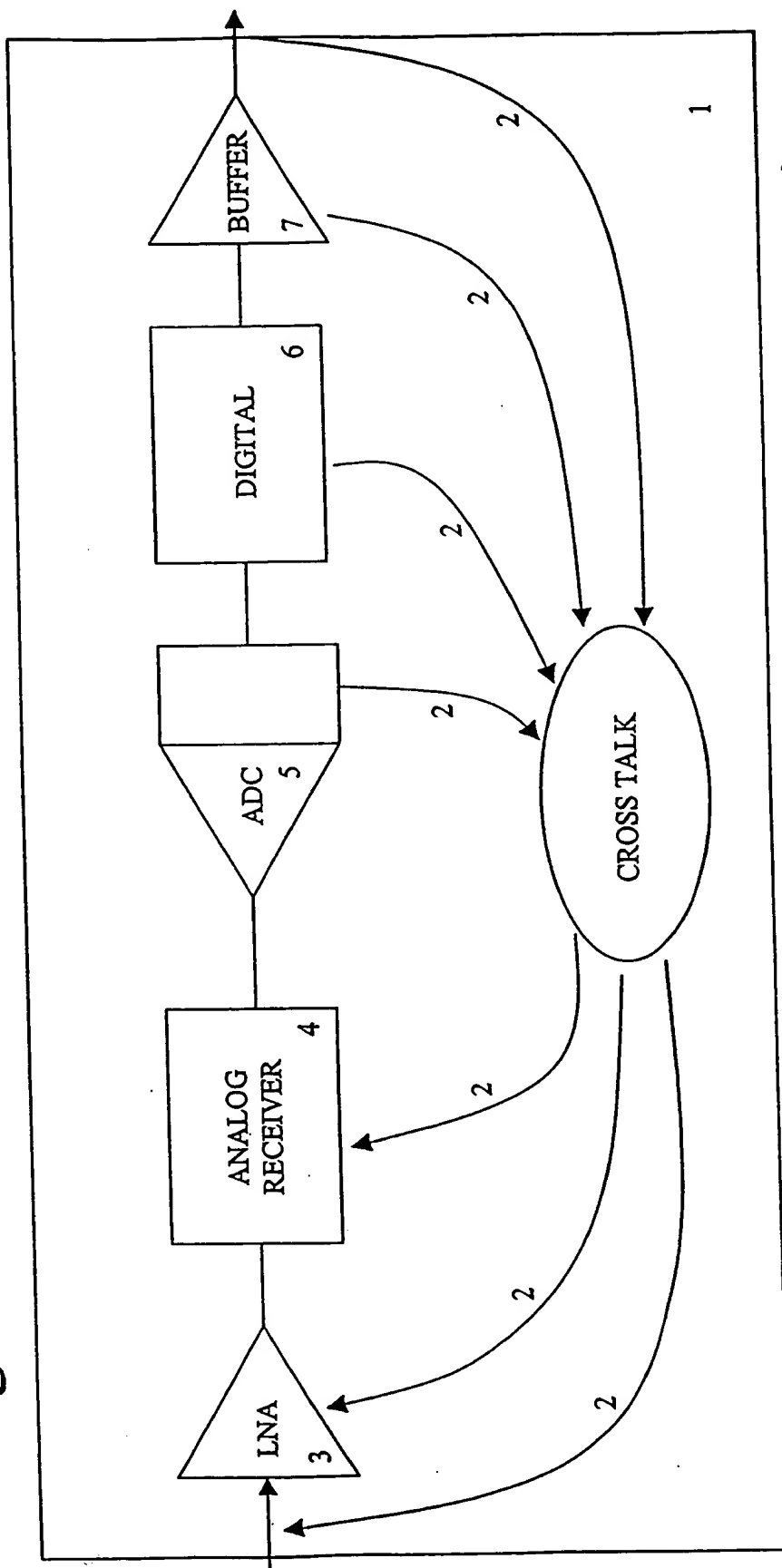
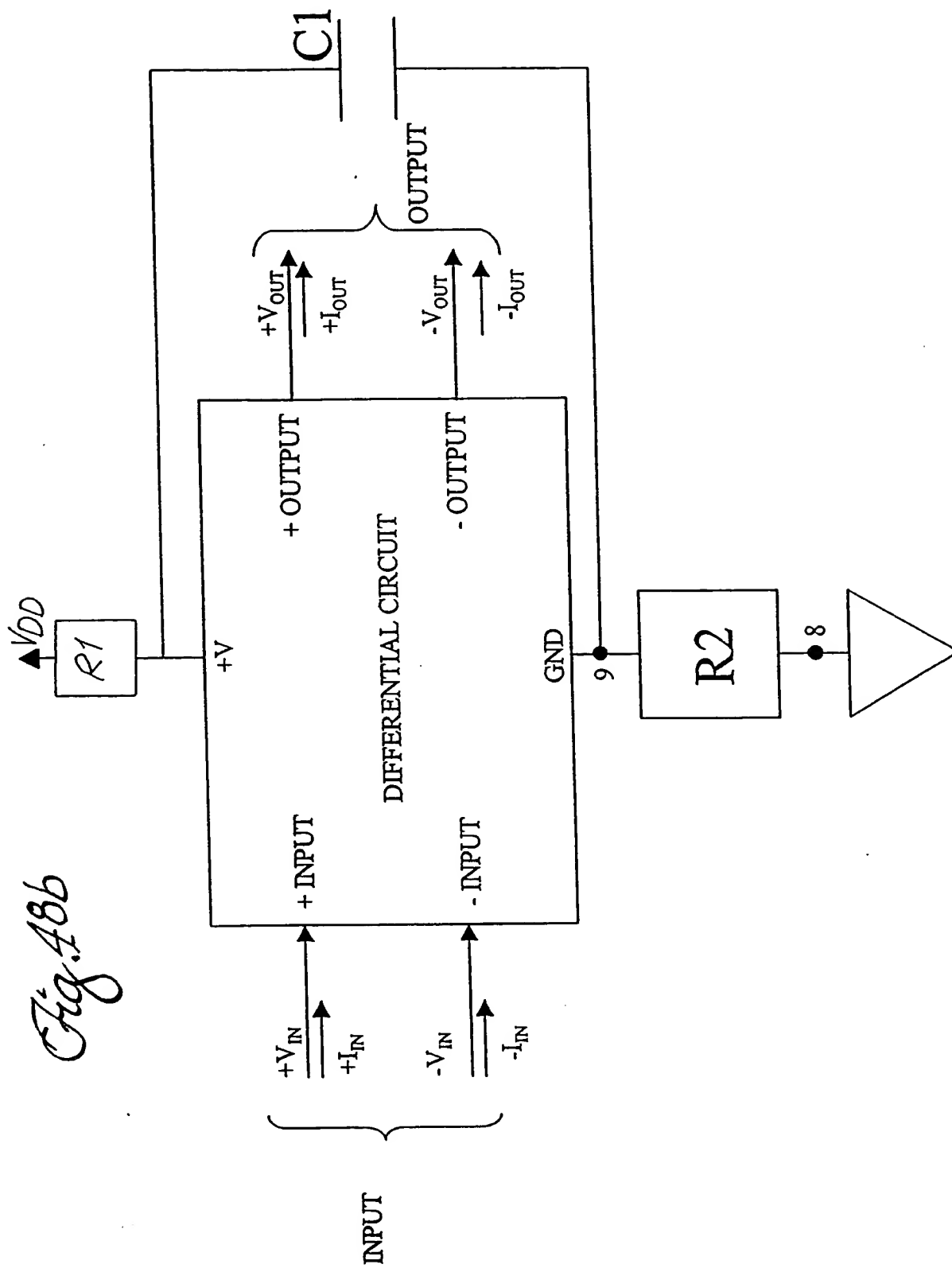
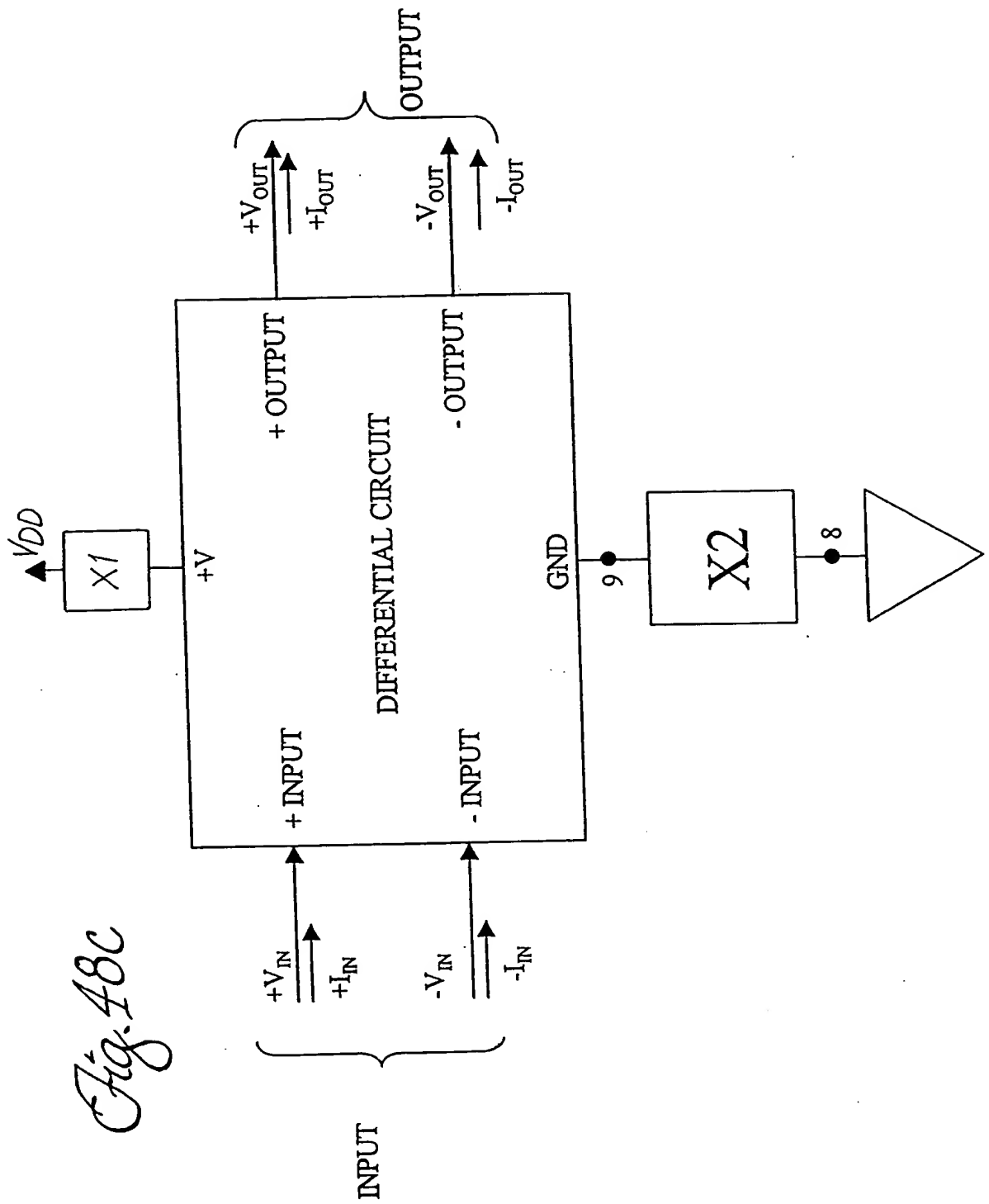
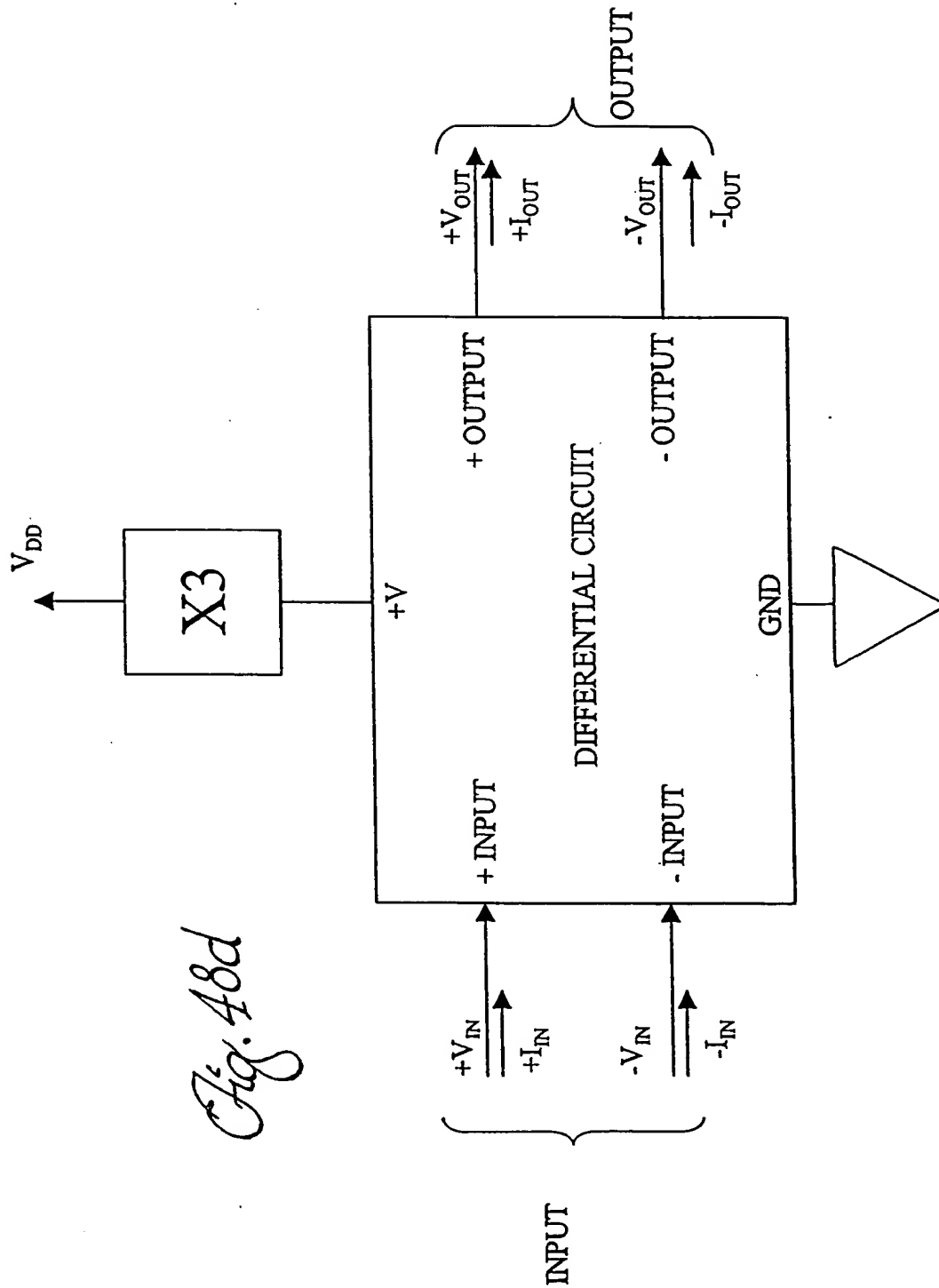


Fig. 48a









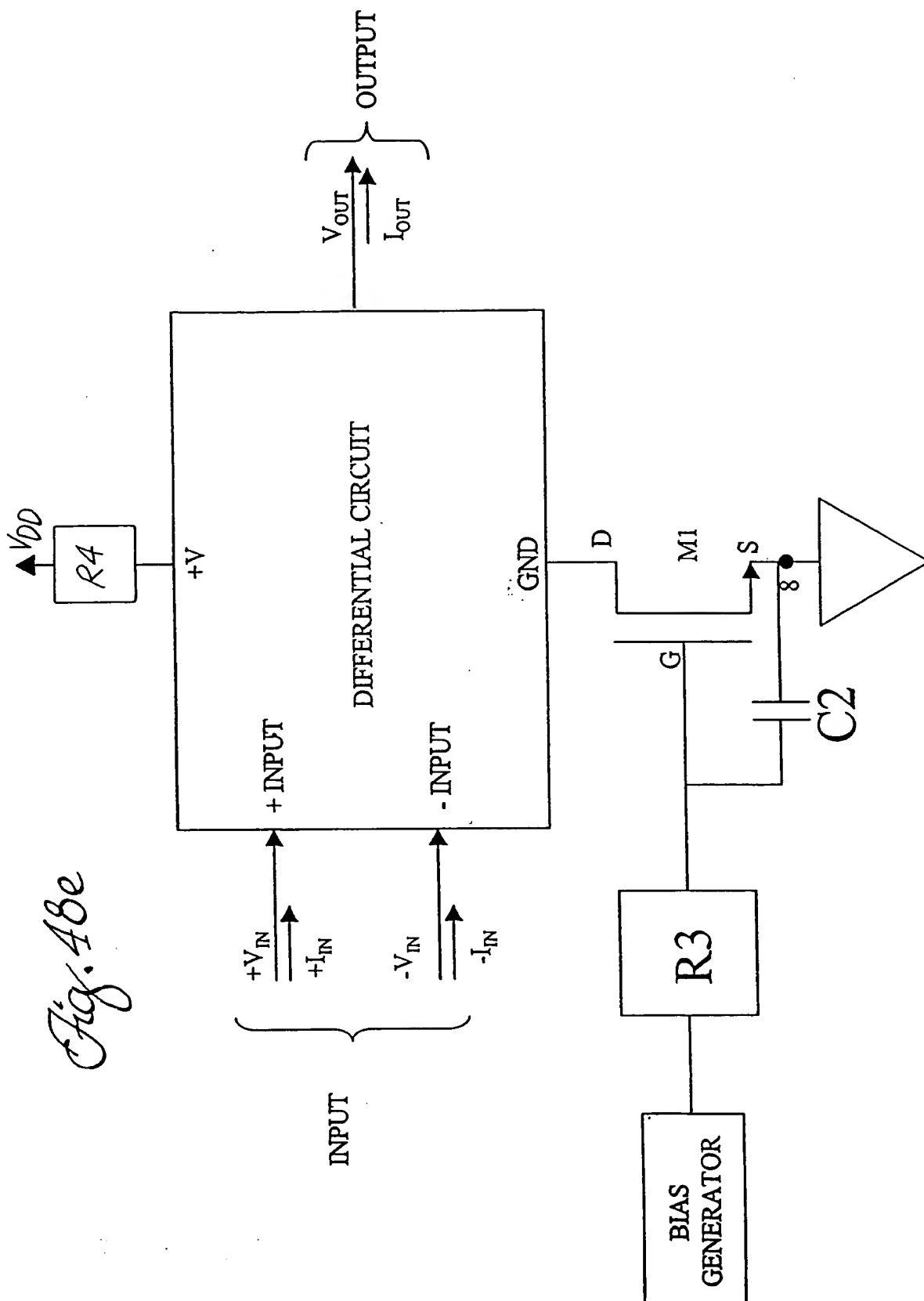


Fig. 48e

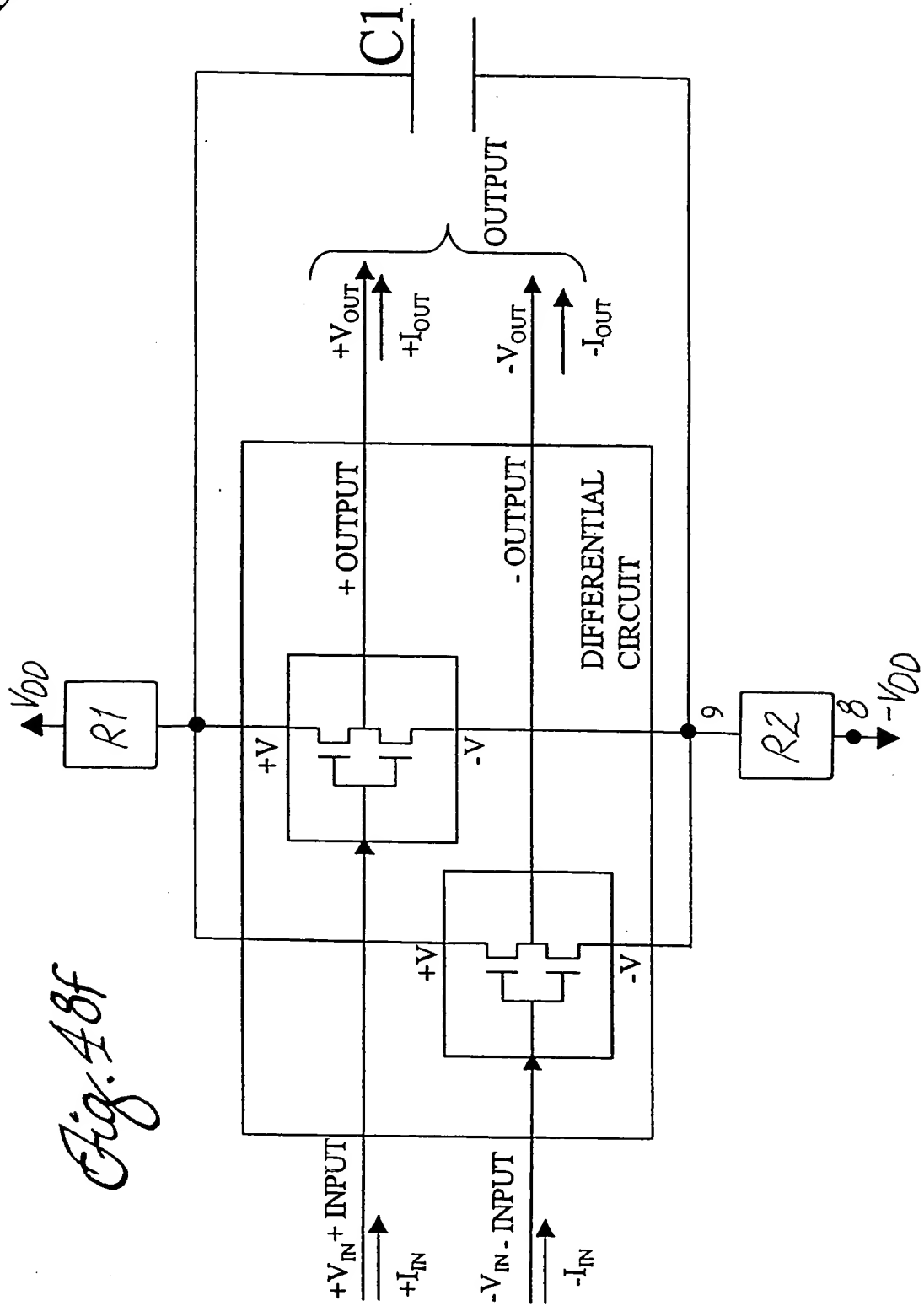


Fig. 48f